DATA TRANSLATION

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DT9840 Series
User's Manual

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Radio and Television Interference

This equipment has been tested and found to comply with CISPR EN55022 Class A and EN50082-1 (CE) requirements and also with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Changes or modifications to this equipment not expressly approved by Data Translation could void your authority to operate the equipment under Part 15 of the FCC Rules.

Note: This product was verified to meet FCC requirements under test conditions that included use of shielded cables and connectors between system components. It is important that you use shielded cables and connectors to reduce the possibility of causing interference to radio, television, and other electronic devices.

Canadian Department of Communications Statement

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class A prescrites dans le Règlement sur le brouillage radioélectrique édicté par le Ministère des Communications du Canada.

Table of Contents

About this Manual

This manual describes the hardware features of the DT9840 Series modules.

Intended Audience

This document is intended for engineers, scientists, technicians, or others responsible for using and/or programming the DT9840 Series modules for data acquisition operations in the Microsoft® Windows® 2000 or Windows XP operating system. It is assumed that you have familiarity with data acquisition principles and that you understand your application.

How this Manual is Organized

This manual provides detailed information about the operation of the DT9840 Series modules. It is organized as follows:

- Chapter 1, "Principles of Operation," describes the system features and the features of the analog input, analog output, digital I/O, and counter/timer subsystems.
- Chapter 2, "Register Description," describes all the registers that are used to program the DT9840 Series modules.
- Chapter 3, "Calibration," describes the DT9841 Calibration Utility.
- Appendix A, "Specifications," lists the specifications of the module.
- Appendix B, "Connector Pin Assignments," shows the pin assignments for the connectors and the screw terminal assignments for the module.
- An index completes this manual.

Conventions Used in this Manual

The following conventions are used in this manual:

- Notes provide useful information or information that requires special emphasis, cautions provide information to help you avoid losing data or damaging your equipment, and warnings provide information to help you avoid catastrophic damage to yourself or your equipment.
- Items that you select or type are shown in **bold**.

Related Information

Refer to the following documents for more information on using the DT9840 Series modules:

- *Benefits of the Universal Serial Bus for Data Acquisition*. This white paper describes why USB is an attractive alternative for data acquisition. It is available on the Data Translation web site (www.datatranslation.com).
- *DT9840 Series Getting Started Manual* (UM-19199). This manual, included on the DT9840 Series Software CD, describes the how to install the DT9840 Series modules and related software.
- *DT9840 Series DSP Library User's Manual* (UM-19591). This manual, included on the DT9840 Series Software CD, describes how to write a DSP program for the DT9840 Series modules.
- *DT9840 Series Host Communication Library User's Manual* (UM-19593). This manual, included on the DT9840 Series Software CD, describes how to write a host application program that communicates with the DSP program running on the DT9840 Series module.
- Documentation for Code Composer Studio™ Integrated Development Environment (IDE) from Texas Instruments.

- Documentation for Texas Instruments TMS320C6713 DSP processor.
- Microsoft Windows 2000 or Windows XP documentation.
- Microsoft Visual Studio documentation.
- USB 1.1 and USB 2.0 specifications on the USB web site (http://www.usb.org).

Where to Get Help

If you have difficulty using a DT9840 Series module, Data Translation's Technical Support Department is available to provide technical assistance.

To request technical support, go to our web site at http://www.datatranslation.com and click on the Support link.

When requesting technical support, be prepared to provide the following information:

- Your product serial number
- The hardware/software product you need help on
- The version of the CD you are using
- Your contract number, if applicable

If you are located outside the USA, contact your local distributor; see our web site (www.datatranslation.com) for the name and telephone number of your nearest distributor.

1

Principles of Operation

DT9840 Series modules provide simultaneous analog I/O, digital I/O, and counter/timer operations on the USB bus. The hardware design features an embedded Texas Instruments TMS320C6713 DSP processor that manages I/O functions on the module. This 300 MHz processor provides float-point functionality and supports standard programming tools from Texas Instruments, including Code Composer Studio.

Data Translation provides a library of DSP functions that you can use within a standard Code Composer program to access the functionality of the DT9840 Series modules, as well a library of communication functions that you can use to communicate between a DT9840 Series module and a Windows-based host program. Refer to the *DT9840 Series DSP Library User's Manual* and *DT9840 Series Host Communications Library User's Manual* for more information about the functions included in these libraries. For maximum flexibility, you can also program your own digital signal processing tasks at the DSP-level, if you wish.

Currently, the DT9840 Series consists of the DT9841, DT9841E, DT9841-VIB, DT9842/2, and DT9842/8 modules. Table 1 describes the differences among the modules.

Table 1: DT9840 Series Modules

Models	Analog Inputs	Converter Type	Resolution	Sampling Rate	Analog Filtering	Analog Outputs	Scalable Bus
DT9841	8DI[a]	Delta-Sigma	24-bit[b]	200 Hz to 100 kHz	Yes[c]	2[d]	Yes
DT9841-VIB[e]	8SE[a]	Delta-Sigma	24-bit[b]	200 Hz to 100 kHz	Yes[c]	2[d]	Yes

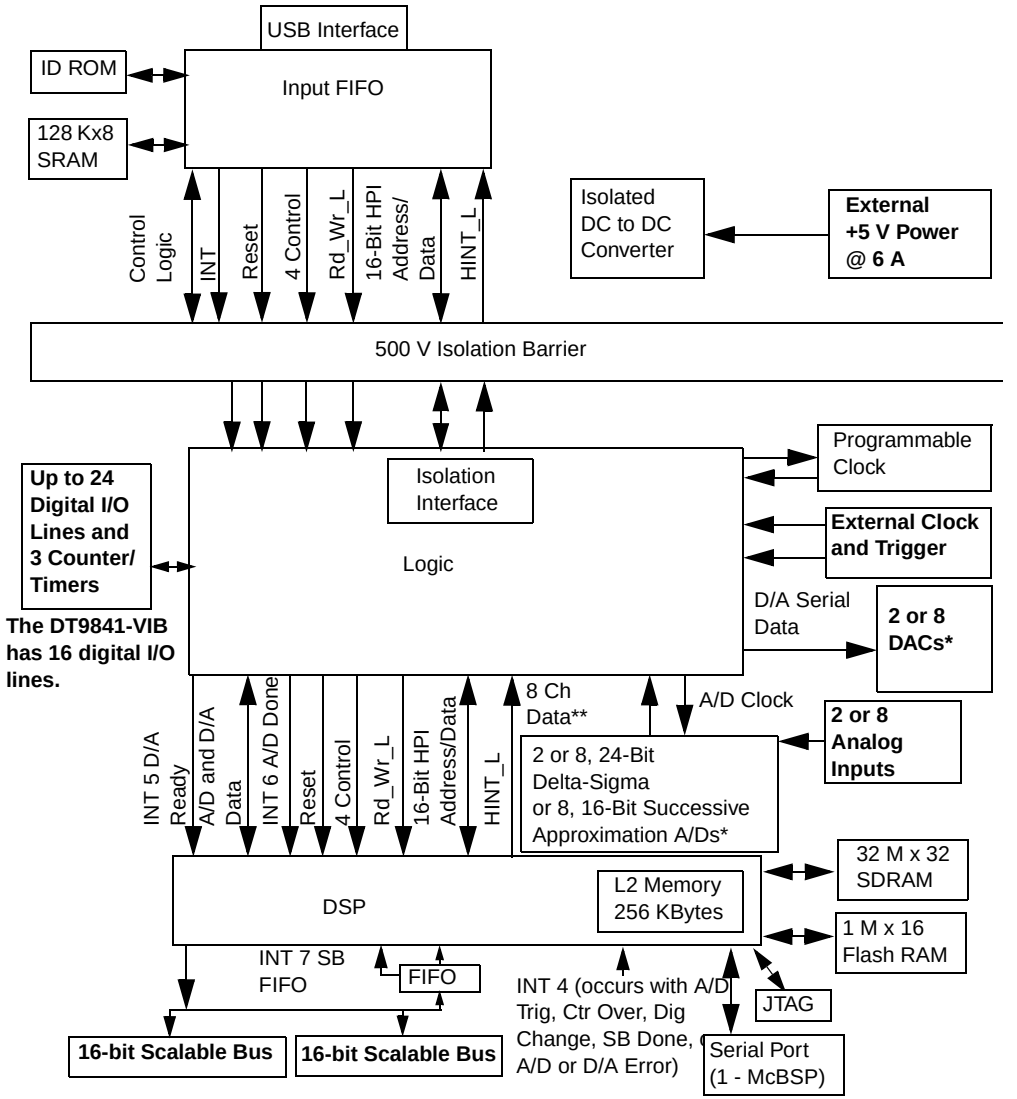
Table 1: DT9840 Series Modules (cont.)

Models	Analog Inputs	Converter Type	Resolution	Sampling Rate	Analog Filtering	Analog Outputs	Scalable Bus
DT9841 E	2DI[a]	Delta-Sigma	24-bit[b]	200 Hz to 100 kHz	Yes[c]	2[d]	No
DT9842 /2	8SE[a]	Successive Approximation	16-bit[b]	0 Hz to 100 kHz	No	2[f]	Yes
DT9842 /8	8SE[a]	Successive Approximation	16-bit[b]	0 Hz to 100 kHz	No	8[f]	Yes

a. DI refers to differential mode and SE refers to single-ended mode. For differential inputs only, you can configure the termination resistance in software on a channel-by-channel basis.
b. The input signal range is ±10 V.
c. Software-selectable output filters of 5 kHz and 20 kHz are available.
d. Software-selectable output ranges of ±10 V and ±2.5 V are available.
e. The DT9841-VIB supports IEPE functions on the analog input channels. The DT9841-VIB module has two 8-bit digital I/O ports, where the standard DT9841 product has three 8-bit digital I/O ports.
f. The output signal range is ±10 V.

This chapter describes the operation of the DT9840 Series modules from a hardware perspective. Figure 1 shows a block diagram of the DT9840 Series hardware architecture to frame the discussion in this chapter. Note that bold entries indicate signals you can access.

For more detailed, register-level information, refer to Chapter 2 starting on page 65.



*** The DT9841 and DT9841-VIB features 8, 24-bit A/Ds and 2, 24-bit DACs.**
The DT9841E features 2, 24-bit A/Ds and 2, 24-bit DACs.
The DT9842/2 features 8, 16-bit A/Ds and 2, 16-bit DACs.

****This is serial on the DT9841, DT9841E, and DT9841-VIB, and parallel on the DT9842/2 and DT9842/8.**

Figure 1: Block Diagram of the DT9840 Series Modules

System Features

The DT9840 Series modules provide the following system-level features:

- Memory, described below
- Clock sources, described on page 18
- Conversion modes, described on page 22
- Triggers, described on page 27
- Connections for multiple modules, described on page 29
- LEDs, described on page 31

Memory

All DT9840 Series modules provide 128 MB of onboard SDRAM and 2 MB of flash memory. Flash memory is divided into two sections: a single 64 KB block is reserved for user data; the remaining memory (2 MB – 64 KB) is reserved for storing a DSP program

You can download a program into SDRAM using the DT9840 Series Download Utility, described in the *DT9840 Series Getting Started Manual*, and then run and debug the program.

Once you have debugged the program, you can store it in flash memory using the DT9840 Series Flash Download Utility, described in the *DT9840 Series Getting Started Manual*. This allows the DSP program to run automatically each time the DT9840 Series module is powered on, autonomously from the PC.

If desired, you can also copy a user data fie into flash memory using the DT9840 Series Flash Download Utility. By copying a user data into flash, you can ensure that valuable information, such as configuration information or collected data, persists across power cycles, even if the DT9840 Series module loses power or is turned off.

Notes: Only one DSP program can be running on a module at one time. In addition, only one user data file can be stored in flash memory at a time.

Each DT9840 Series module also requires a CDB file for proper operation. Refer to the *DT9840 Series DSP Library User's Manual* for more information on CDB files.

Clock Sources

DT9840 Series modules support the following sample clock sources:

- Internal clock, described below
- External clock, described on page 20
- Scalable Bus master clock, described on page 21

Internal Clock

The internal clock has a 36 MHz time base for the DT9841, DT9841E, and DT9841-VIB modules and an 18 MHz time base for the DT9842/2 and DT9842/8 modules. Conversions start on a high-to-low transition after a rising edge of the internal calibration signal.

Use software to specify the internal clock source and the frequency at which to pace the input and output operations and to start the sample clock. For the DT9841, DT9841E, and DT9841-VIB, the sampling frequency ranges from 200 Hz to 100 kHz. For the DT9842/2 and DT9842/8, the sampling frequency ranges from 0 Hz to 100 kHz.

Note: According to sampling theory (Nyquist Theorem), specify a frequency that is at least twice as fast as the input's highest frequency component. For example, to accurately sample a 20 kHz signal, specify a sampling frequency of at least 40 kHz to avoid aliasing.

The actual frequency that the module can achieve may be slightly different than the frequency you specified due to the accuracy of the clock (0.01% for the DT9840 Series). You can determine the actual clock frequency using software.

DT9841, DT9841E, and DT9841-VIB Internal Clock

On the DT9841, DT9841E, and DT9841-VIB modules, the value that you specify for the internal clock frequency is multiplied by 512 internally to set the oscillator on the module. The resulting signal from the oscillator is then divided by 2 to provide a clock signal to the A / D and D / A converters that is oversampled 256 times and has a 50% duty cycle. For example, if you specify an internal clock frequency of 100 kHz, internally the module sets the oscillator to 51.2 MHz then divides the resulting signal by 2 to provide a 25.6 MHz signal with a 50% duty cycle to the A / D and D / A converters.

In addition, if you specify a sampling frequency between 200 Hz and 5 kHz, the DT9841, DT9841E, and DT9841-VIB modules automatically filter the data using decimation and interpolation filters. Refer to the *DT9840 Series DSP Library User's Manual* for more information on how these filters are implemented.

Once the sample clock is started, the DT9841, DT9841E, and DT9841-VIB modules require 37 clock pulses before the first conversion is completed (at 100 kHz, this delay is 370 µs). Thereafter, the data is converted without delay (at 100 kHz, sampling occurs every 10 µs). This initial delay is required by the filtering algorithms of the A/D and D/A converters.

DT9842/2 and DT9842/8 Internal Clock

Because the DT9842/2 and DT9842/8 use successive-approximation A/D converters and provides no inherent filtering, no initial delay occurs (like on the DT9841, DT9841E, and DT9841-VIB). Therefore, the converter always runs as fast as possible (at 100 kHz, sampling occurs every 10 µs).

Internally, the DT9842/2 and DT9842/8 hardware divides the 18 MHz time base by a 32-bit value to achieve the closest rate to the sampling rate you requested.

External Clock

An external clock is useful when you want to pace acquisitions at rates not available with the internal sample clock or when you want to synchronize a DT9840 Series module with other devices in your system.

For the DT9841E module, connect the external clock to pin 23 of connector J1. For all other modules, connect the external clock to the Ext Clk BNC input on the module. Use software to specify the external clock source and to start the sample clock. Conversions start on a high-to-low transition of the external clock signal after a rising edge of the internal calibration signal.

DT9841, DT9841E, and DT9841-VIB External Clock

For the DT9841, DT9841E, and DT9841-VIB, ensure that the external clock source has a 50% duty cycle. The resulting frequency of the external clock input is equal to the frequency of the external clock signal that you connected to the module divided by 256 (this division is done internally by the module), and must be in the range of 200 Hz to 100 kHz. For example, if you need a sampling frequency of 100 kHz, use an external clock source with a frequency of 25.6 MHz.

Once the external clock is started, the DT9841, DT9841E, and DT9841-VIB modules require 37 clock pulses before the first conversion is completed (at 100 kHz, this delay is 370 µs). Thereafter, the data is converted without delay (at 100 kHz, sampling occurs every 10 µs). This initial delay is required by the filtering algorithms of the A/D and D/A converters.

DT9842/2 and DT9842/8 External Clock

Because the DT9842/2 and DT9842/8 use successive-approximation A/D converters and provide no inherent filtering, no initial delay occurs (like on the DT9841, DT9841E, and DT9841-VIB). Therefore, the resulting frequency of the external clock input is equal to the frequency of the external clock signal that you connected to the module.

Scalable Bus Master Clock

Note: The Scalable Bus is not supported by DT9841E modules.

Use the Scalable Bus Master Clock source only if you are using the Scalable Bus to connect multiple modules and you want to synchronize their operation. Refer to page 29 for more information on Scalable Bus operations.

In this configuration, the clock, internal trigger, and reset signals are provided to the slave modules from the master DT9840 Series module through the Scalable Bus. You can configure the master module to use either an internal or external clock source. The Ext Clk BNC connector on the slaves is not used.

Operation Modes

DT9840 Series modules support the following operation modes:

- Single value, described below
- Single scan, described on page 23
- Multiple scan input, described on page 24
- Function generator output, described on page 24
- Continuous loop operations (scan loop, block loop, and list loop), described on page 25

Single-Value Operations

Use software to perform a single-value operation. A DT9840 Series module acquires one value from a specified channel or outputs one value to a specified channel on the next pulse of the sample clock, and then stops. Triggers are ignored.

You can acquire data from an analog input channel, digital input line, or counter/timer channel.

You can output data to either an analog output channel or a digital output line.

Single-Scan Operations

Use software to perform a single-scan operation. A DT9840 Series module acquires one input scan record and / or outputs one output scan record on the next pulse of the sample clock, and then stops. Triggers are ignored.

An input scan record consists of the following information:

- Eight analog input values corresponding to analog input channels 0, 1, 2, 3, 4, 5, 6, and 7. For the DT9841, DT9841E, and DT9841-VIB, these are 24-values; for the DT9842, these are 16-bit values.

Note: The DT9841E supports only two analog input channels (0 and 1). Therefore, values for channels 2 through 7 in the input scan record should be ignored.

- One 24-bit value corresponding to all the digital input lines. For the DT9841-VIB, only 16-bits (ports 0 and 1) are accessible.
- One 32-bit value containing the state of the digital input lines. For the DT9841-VIB the least significant 16-bits of this 32-bit value correspond to the digital inputs of port 0 and port 1. On all other DT9840 Series modules, the least significant 24-bits of this 32-bit value correspond to the digital inputs of port 0, port 1 and port 2.
- Three 32-bit values corresponding to counter / timer channels 0, 1, and 2.

An output scan record consists of the following information:

- For the DT9841, DT9841E, and DT9841-VIB, two 24-bit values corresponding to analog output channel 0 and 1. For the DT9842/2, two 16-bit values corresponding to analog output channel 0 and 1. For the DT9842/8, eight 16-bit values corresponding to analog output channels 0 to 7.
- One 24-bit value corresponding to all the digital output lines.

Multiple-Scan Input Operations

Use software to perform a multiple-scan input operation. When it detects a trigger event, the DT9840 Series module acquires a specified number of input scan records, and then stops. An input scan record is acquired on each pulse of the sample clock.; refer to page 23 for more information on input scan records.

This is a synchronous operation; therefore, you cannot perform any other operation while this operation is in process.

Function Generator Output Operations

Use software to start a function generator output operation. When it detects an initial trigger, the DT9840 Series module outputs a buffer that contains a specified number of output scan records. Refer to page 23 for more information on output scan records.

The module continuously outputs the data in the output scan records from the buffer in memory to the analog output channels and/or digital output lines on each pulse of the sample clock. Once the operation is started, the DSP is not used.

When you are finished outputting the data, use software to stop the operation.

Continuous Loop Operations

DT9840 Series modules support three types of continuous loop operations:

- Scan loop operations, described below
- Block loop operations, described on page 26
- List loop operations, described on page 26

The most appropriate mode depends on your application.

Use scan loop mode in control loops and other applications where you need to acquire a sample on every tick of the sample clock and process the data as soon as possible. This mode is less efficient than block loop and list loop operations, but allows more timely access to the data.

Block and list loop operations process data in blocks. Your program gets called only when an entire block of data has been acquired. These modes are more efficient than scan loop, but give less frequent access to the incoming data.

Block and list loop operations are very similar in operation. The main difference is that block loop uses only two block buffers, which are automatically allocated and managed, while list loop uses a linked list of as many buffers as you want, but your program must allocate and free each buffer appropriately.

Scan Loop Operations

Use software to start a scan loop operation. When it detects a trigger event, the module continuously acquires an input scan record and / or outputs an output scan record on each pulse of the sample clock, until you stop the operation. Refer to page 23 for more information on input and output scan records.

The sample rate is determined by the frequency of the sample clock and is the rate at which a single input scan record is acquired and a single output scan record is output; refer to page 18 for more information on the sample clock.

Block Loop Operations

Use software to start a block loop operation. When it detects a trigger event, the module continuously acquires input blocks and / or outputs output blocks until you stop the operation.

Each input block consists of the following information:

- Input scan records; refer to page 23 for more information on input scan records
- The number of scans in each block
- A flag that indicates whether or not the block is full
- A pointer to the next block

Each output block consists of the following information:

- Output scan records; refer to page 23 for more information on output scan records
- The number of scans in each block
- A flag that indicates whether or not the block is full
- A pointer to the next block

List Loop Operations

To perform a list loop operation, use software to allocate a linked list of input and / or output blocks, and start the list loop operation. When it detects a trigger event, the module acquires lists of input blocks and / or outputs lists of output blocks. Each list contains a specified number of input and / or output blocks. Refer to page 26 for more information on input and output blocks.

You can specify whether to stop the operation when the number of blocks have been filled (for an input operation) or emptied (for an output operation) or whether to continue the operation starting by overwriting the first block in the list.

When you are finished acquiring and/or outputting data, you can use software to stop a continuous operation and free the previously allocated memory.

Triggers

A trigger is an event that occurs based on a specified set of conditions. Using software, you can specify these conditions by selecting one of the following trigger sources:

- **Software trigger** – The trigger event occurs immediately when you start the operation (the computer issues a write to the module to begin conversions).

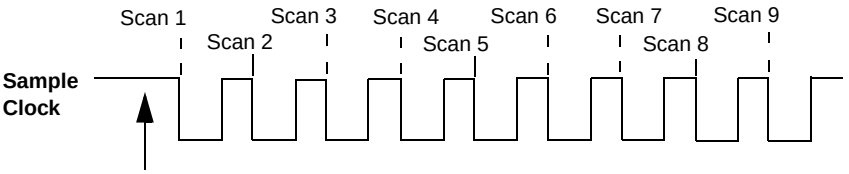
Note: If you are using the Scalable Bus to connect multiple modules and you want to use an internal trigger to trigger the master and slave modules, no extra wiring is required. The internal trigger signal is provided to the slave modules through the Scalable Bus cables and connectors. Refer to page 29 for more information on using the Scalable Bus.

- **External trigger** – The trigger event occurs when the module detects a low to high transition on the TTL-level signal connected to the external input of the module. For the DT9841E module, connect the external trigger to pin 24 of connector J1. For all other modules, connect the external trigger to the Ext Trig BNC on the module. This trigger asserts EXT_INT4 for processing.

Note: If you are using the Scalable Bus to connect multiple modules and you want to externally trigger the master and slave modules at the same time, you must supply an external trigger signal to the master and each slave module using external wiring. The external trigger signals is not provided through the Scalable Bus cable and connectors. Refer to page 29 for more information on using the Scalable Bus.

When the DT9840 Series module detects the specified trigger event, the input and / or output operation starts at the clock frequency of the specified clock source.

Figure 2 illustrates acquisition using an external trigger source. In this example, an input scan record is acquired on each pulse of the selected clock source when the external trigger event occurs.



The module detects a low-to-high transition on the TTL-level signal attached to the Ext Trig BNC. Data is acquired on each pulse of the sample clock.

Figure 2: Acquisition Using an External Trigger

Notes: Because the DT9841, DT9841E, and DT9841-VIB modules require 37 clock pulses before the first analog input conversion is completed, the first 37 analog samples that are acquired after the trigger are actually pre-trigger samples. The 38th sample corresponds to the first data point after the trigger. Digital input and counter/timer data is always acquired immediately after the trigger and is not delayed by 37 samples

Since the DT9842/2 and DT9842/8 do not have a group delay, the samples acquired after the trigger correspond directly to the data that was acquired.

Triggers are ignored for single-value operations and single-scan operations. These operations are performed immediately after the functions are executed.

Scalable Bus

Note: The Scalable Bus is not supported by DT9841E modules.

The architecture of the DT9840 Series supports connecting up to eight modules together through the Scalable Bus; one of the modules is the master and the remaining modules are slaves. This connection scheme allows you to synchronize the operation of all modules at the frequency of the master clock source, or to communicate with multiple modules that are operating asynchronously from each other.

The modules connect together using EP342 cables and the 50-pin Scalable Bus connectors (J12 and J13). Refer to the *DT9840 Series Getting Started Manual* for more information on connecting modules using the Scalable Bus connectors.

Using the DT9840 Series Control Panel application, you must enable the Scalable Bus, assign a unique address for each module on the bus, and configure the final slave module on the bus with 100 Ω termination. Refer to the *DT9840 Series Getting Started Manual* for more information on using the DT9840 Series Control Panel application.

If you want to synchronize the operation of all modules connected on the Scalable Bus, do the following:

1. Configure the master module to use either an internal or external clock source. If you select an external clock, ensure that you attach a clock signal to the Ext Clk BNC connector on the master module.
2. Set the clock source for each slave module to AD_DA_CLK_SRC_SB_MASTER using the **DT_SetupClock** function. The clock and reset signals are provided to all the slave modules from the master DT9840 Series module through the Scalable Bus cables and connectors. In this configuration, the Ext Clk BNC connector on the slave modules is not used.
3. Configure the master module to use either an internal or external trigger source. The Scalable Bus cables and connectors provide the internal trigger signal (but not the external trigger signal) from the master module to the slave modules. Therefore, if you are using an internal trigger to trigger the master and slave modules, the Ext Clk BNC connector on the slave modules is not used.

   If you select an external trigger, ensure that you attach a trigger signal to the Ext Trig BNC connector on the master module and to the Ext Trig BNC connector on each slave module.

Refer to the *DT9840 Series Getting Started Manual* for more information on attaching signals.

For asynchronous operation, you can set the clock source for both the master and slave modules to either internal or external (but not to Scalable Bus master). Each module is then clocked and triggered separately; you can communicate with all the modules on the bus using software.

You can perform the following communication operations on the Scalable Bus using software:

- Return the address of slave modules
- Determine whether the module is ready for data transfer
- Allocate and deallocate buffers for data transfer
- Initiate transfer requests from the slave
- Transfer data and messages from the master to the slave

LEDs

LED CR6 on the DT9841E module and LED CR1 on the back of all other DT9840 Series modules is a two-color device that indicates the state of the DT9840 Series module. Refer to the *DT9840 Series Getting Started Manual* for the location of this LED.

When power is applied to the module, this LED turns green. When the module is recognized by the host and the firmware is downloaded to the module, the LED turns red. When the Windows driver is loaded and started, the LED turns orange. The module is then ready for use.

When you download and run your DSP program, this LED flashes green and orange. If the downloaded program stops running, this LED turns stops flashing (in either the green or orange state) to indicate that an error occurred, and the debug LEDs (CR7 to CR14) turn on. You can define the state of the debug LEDs using software.

Note: Debug LEDs are not supported on DT9841E modules.

Analog Input Features

This section describes the following features specific to the analog input (A/D) subsystem:

- Analog input channels, described below
- IEPE functions, described on page 33
- Input resolution, described on page 34
- Input range and gain, described on page 34
- Data formats, described on page 35
- Data transfer, described on page 35
- Error conditions, described on page 36

Analog Input Channels

The DT9841E modules support two analog input channels (numbered 0 and 1). All other DT9840 Series modules support eight analog input channels (numbered 0 to 7). All analog input channels are simultaneously clocked. On the DT9841 and DT9841E, these channels are configured as differential inputs; on the DT9841-VIB, DT9842/2, and DT9842/8, these channels are configured as single-ended inputs.

The DT9841, DT9841E, and DT9841-VIB use Delta-Sigma analog-to-digital converters (ADCs) that provide anti-aliasing filters (down to 200 Hz) based on the clock rate. These filters remove *aliasing*, which is a condition where high frequency input components erroneously appear as lower frequencies after sampling.

The DT9842/2 and DT9842/8 use successive approximation converters (no filtering is supported).

Using software, you can configure the DT9841 and DT9841E modules to use 1 kΩ bias return termination resistance between the low side of each differential channel and isolated analog ground. This feature is particularly useful with floating signal sources. Refer to the *DT9840 Series Getting Started Manual* for more information on wiring to inputs to use bias return termination resistance.

IEPE Functions

The DT9841-VIB module supports the following IEPE functions for each of the eight analog inputs:

- Current source – Using the DSP library, you can enable or disable the use of a 4 mA current source.
- AC/DC coupling – Using the DSP library, you can select whether AC coupling or DC coupling is used.
- Filtering – Using the DSP library, you can enable or disable the use of the 2-pole, 10 kHz, Butterworth filter.

Figure 3 shows a block diagram of the IEPE functions on one of the analog input channels.

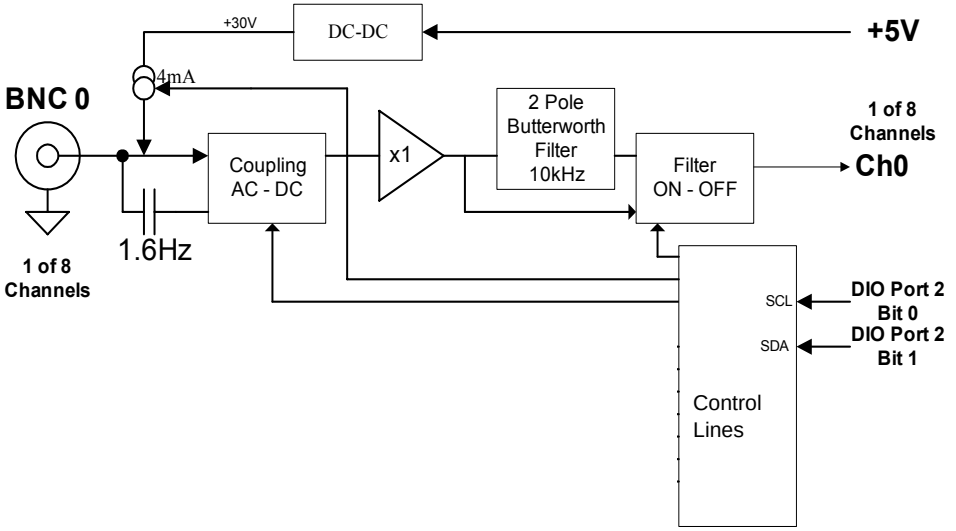


Figure 3: IEPE Block Diagram on the DT9841-VIB

Input Resolution

The input resolution of the DT9841, DT9841E, and DT9841-VIB modules is fixed at 24-bits. The input resolution of the DT9842/2 and DT9842/8 modules is fixed at 16-bits.

Input Range and Gain

All DT9840 Series modules provide an input range of ±10 V and a fixed gain of 1.

Data Format

The analog input data encoding used by the DT9841, DT9841E, and DT9841-VIB modules is floating point. The data is 32-bit wide and left justified; the right eight bits are filled with zeros.

The DT9842/2 and DT9842/8 modules use twos complement data encoding. The data is 32-bit wide and left justified; the right 16 bits are filled with zeros.

Note: When the module is above range, the value FFFFh (plus full-scale) is returned. When the module is below range, the value 0000h (minus full-scale) is returned.

You can use software to convert a twos complement code into voltage.

Data Transfer

DT9840 Series modules generate an interrupt (EXT_INT6) when the A/D conversions are complete. The input samples are loaded into the input FIFO for future transmission over the USB bus to host memory or for onboard digital signal processing. All samples must be read from the FIFO before the next A/D conversion is done.

Error Conditions

DT9840 Series modules report an overrun error if the data from the previous A / D conversion is not read by the DSP or host computer before a new A / D conversion occurs. The DSP or host computer must clear this error.

To avoid this error, ensure that the host program reads data from the module as fast as it is being acquired.

Analog Output Features

This section describes the following features specific to the analog output (D / A) subsystem:

- Analog output channels, described below
- Output resolution, described on page 38
- Output range and gain, described on page 38
- Output filters, described on page 38
- Data format, described on page 39
- Data transfer, described on page 39
- Error conditions, described on page 40

Analog Output Channels

The DT9841, DT9841E, DT9841-VIB, and DT9842 / 2 modules support two analog output channels (0 and 1) that are simultaneously clocked. The DT9842 / 8 module supports eight analog output channels (0 to 7).

On the DT9841, DT9841E, and DT9841-VIB modules, these analog output channels use Delta-Sigma digital-to-analog converters (DACs) that provide anti-aliasing filters based on the clock rate to reduce noise. On the DT9842 / 2 and DT9842 / 8, these analog output channels use successive approximation DACs (no filtering is supported).

Within each DAC, the digital data is double-buffered to prevent spurious outputs before it is output as an analog signal. Both DACs power up to a value of 0 V ±10 mV. Resetting the module does not clear the values in the DACs.

Refer to the *DT9840 Series Getting Started Manual* for information on how to wire analog output signals to the module.

Output Resolution

The output resolution of the DT9841, DT9841E, and DT9841-VIB modules is fixed at 24 bits. The output resolution of the DT9842/2 and DT9842/8 modules is fixed at 16 bits.

Output Range and Gain

Each analog output channel on a DT9841, DT9841E, or DT9841-VIB module can output bipolar analog output signals in the range of ±10 V or ±2.5 V. The output range is software-selectable. The gain is fixed at 1.

The DT9842/2 and DT9842/8 modules support an output range of ±10 V only.

Output Filters

Note: Output filters are supported on the DT9841, DT9841E, and DT9841-VIB modules only.

Each analog output channel on the DT9841, DT9841E, or DT9841-VIB supports a software-selectable four-pole 5 kHz filter or a four-pole 20 kHz filter. Both are Bessel filters and are useful if you want to smooth the analog output values. For fast clock rates, it is recommended that you use the 20 kHz filter. For slow clock rates, it is recommended that you use the 5 kHz filter.

On power-up or reset, no filter is used.

Data Format

The analog output data encoding used by the DT9841, DT9841E, an DT9841-VIB modules is floating point. The data is 32-bit wide and left justified; the right eight bits are filled with zeros.

The DT9842/2 and DT9842/8 modules use twos complement data encoding. The data is 32-bit wide and left justified; the right 16 bits are filled with zeros.

You can use software to convert a voltage value into a twos complement code.

Data Transfer

The module packs 32 bits into each transfer. The board generates an interrupt (EXT_INT5) after the data in the analog output channel has been output. For 100 kHz operation, both analog output channels must then be updated with the next value to write within 10 µs.

For the DT9841, DT9841E, and DT9841-VIB modules, analog output data must always be output as two 32-bit words: channels 0, then channel 1. The data is clocked into the internal serial output register on the second word address. The initial value must be the code for 0 V output to prevent glitching after power up.

For the DT9842/2 and DT9842/8, when new data is written to any of the analog output data registers, all of the analog output channels are updated on the next clock cycle. For example, assume that you write a new value to analog output channel 0. On the next clock cycle, channel 0 is updated with the new value you specified, and all the other analog output channels are updated with the existing values in the corresponding data registers.

Error Conditions

DT9840 Series modules report an analog output underflow error to the host computer if the analog output data is not transferred fast enough (within 10 µs of the fastest clock rate) from the host computer to the module. The host computer must clear this error.

To avoid this error, ensure that the host computer provides analog output data to the module faster than the DACs are converting the data.

Digital I/O Features

This section describes the following features specific to the digital input and digital output subsystems:

- Digital I/O lines
- Interrupts

Digital I/O Lines

The DT9841-VIB module supports two 8-bit ports (ports 0 and 1). All other DT9840 Series modules support three 8-bit ports (ports 0, 1, and 2). You can program these ports for digital input or digital output using software. If you configure port 0 as a digital input port, the interrupt-on-change feature, described in the next section, is available.

On power up or module reset, no digital data is output from the modules. All the outputs include diode protection to the isolated ground and the isolated +5 V.

Interrupt On Change

If port 0 is configured for digital input, the DT9840 Series module can generate an interrupt when any of the lines of port 0 changes state. This feature is useful when you want to monitor critical signals or when you want to signal the host computer to transfer data to or from the module. You specify an interrupt handler using software.

The DT9840 Series modules provide deglitching circuitry that you can enable (using software) for the digital inputs of port 0. If this circuitry is enabled, any state changes that result from noise sources, slow rise or fall times, or switch bounce on the input source are ignored for approximately 10 ms. Deglitching the inputs prevents most situations where multiple interrupts can occur for one state change.

If you are using the interrupt-on-change feature when deglitching is enabled, the maximum frequency that any change can be detected is 500 Hz; if deglitching is disabled, the maximum frequency that any change can be detected is 100 kHz.

Counter/Timer Features

This section describes the following user counter / timer features:

- C / T channels, described below
- C / T clock sources, described on page 43
- Gate types, described on page 45
- Pulse types and duty cycles, described on page 49
- Counter / timer operation modes, described on page 51

C/T Channels

All DT9840 Series modules provide three 32-bit counter / timer channels. The counters are numbered 0, 1, and 2. You select the counter / timer channel to configure using software.

Each counter accepts a clock input signal and gate input signal and outputs a clock output signal (also called a pulse output signal), as shown in Figure 4.

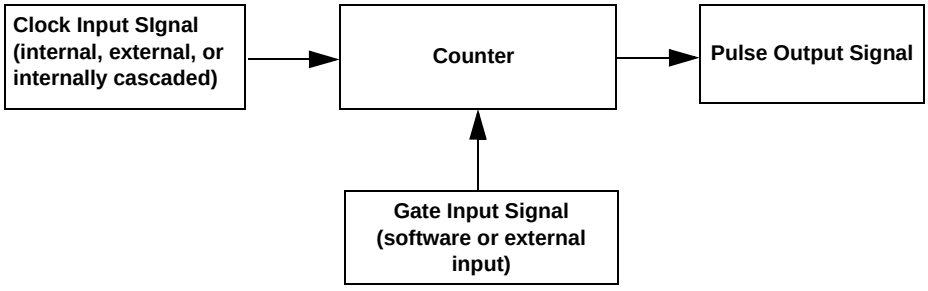


Figure 4: Counter/Timer Channel

C/T Clock Sources

The following clock sources are available for each of the user counter/timers:

- Internal C/T clock
- External C/T clock
- Internally cascaded clock

You specify the clock source to use for the selected counter/timer using software. Refer to the following subsections for more information on each of these clock sources.

Internal C/T Clock

The internal C/T clock uses a 18 MHz time base. Counter/timer operations start on the rising edge of the clock input signal.

External C/T Clock

An external C/T clock is useful when you want to pace counter/timer operations at rates not available with the internal C/T clock or if you want to pace at uneven intervals. Counter/timer operations start on the rising edge of the clock input signal.

Table 2 lists the pin assignments of connector J17 on the module that correspond to the external C/T clock input signals.

Table 2: External C/T Clock Signals on the DT9840 Series Modules

Counter/Timer Signal	J17 Pin Number
User Clock Input 0	6
User Clock Input 1	4
User Clock Input 2	2

Note: For the DT9841-VIB, the clock input signal of counter / timer 0 is also brought out to a BNC on the face plate (CT0 Clock). If you want to use this signal for a tachometer input, ensure that you condition your signal to a TTL input, and configure your counter / timer for continuous measure mode.

Internally Cascaded Clock

You can use software to internally route (or cascade) the clock input signal from a specified counter / timer to the clock output signal of the proceeding counter / timer (without externally connecting two counters together).

For example, if you specify a cascaded clock source for counter / timer 2, the clock input of counter / timer 2 is internally connected to the clock output of counter / timer 1. The C / T clock input source for counter / timer 1 can be an internal or external C / T clock input source, or you can cascade counter / timer 1 to counter / timer 0, if you wish.

The rising edge of the clock input signal is active.

Note: You cannot select a cascaded clock for counter / timer 0, since there is no lower counter / timer with which to cascade.

If you cascade counters, you must read the value of each counter / timer separately and add the values together. For example, if counter / timers 0 and 1 are cascaded, the cascaded count = Ctr 0 + (Ctr1 * 2^{32}).

Gate Types

The active edge or level of the gate input signal of the counter enables counter / timer operations.

Note: The gate type is ignored for measure mode and continuous measure mode operations. Refer to page 55 for more information on measure mode. Refer to page 56 for more information on continuous measure mode.

DT9840 Series modules provide the following gate input types:

- **On** – A software command enables a specified counter / timer operation immediately after execution. This gate type is not supported for up / down counting, one-shot, or repetitive one-shot operations.
- **Normal external gate input** – For standard counting operations, enables the operation when the external gate signal is high, and disables the operation when the external gate signal is low.

  For one-shot and repetitive one-shot operations, enables the operation on the transition from the low level to the high level (rising edge), and disables the operation on the transition from the high level to the low level (falling edge).

  For up / down counting mode, increments the counter when the external gate signal is high, and decrements the counter when the external gate signal is low.

  Refer to page 51 for more information on these modes.

- **Inverted external gate input** – For standard counting operations, enables the operation when the external gate signal is low, and disables the operation when the external gate signal is high.

  For one-shot and repetitive one-shot operations, enables the operation on the transition from the high level to the low level (falling edge), and disables the operation on the transition from the low level to the high level (rising edge).

  For up / down counting mode, increments the counter when the external gate signal is low, and decrements the counter when the external gate signal is high.

Table 3 lists the pin assignments of connector J17 on the module that correspond to the external gate input signals.

Table 3: External Gate Input Signals on the DT9840 Series Modules

Counter/Timer Gate Signal	J17 Pin Number
External Gate 0	39
External Gate 1	37
External Gate 2	35

Edge Types

Note: The edge type applies only to measure mode and continuous measure mode operations.

When measure mode, described on page 55, or continuous measure mode, described on page 56, is selected, you must specify the edge of the signal that starts and stops the measurement.

In measure mode, the counter increments from the specified start edge to the specified stop edge. In continuous measure mode, the counter increments from the specified start edge to the next start edge.

DT9840 Series modules provide the following edge types:

- **Rising-edge external gate input** – In measure mode, starts or stops the measurement when the signal connected to the external gate input pin goes from low to high (rising edge).

  In continuous measure mode, starts the measurement when the signal connected to the external gate input goes from low to high (rising edge); the measurement stops on the next rising edge of the gate signal.

- **Falling-edge external gate input** – In measure mode, starts or stops the measurement when the signal connected to the external gate input pin goes from high to low (falling edge).

  In continuous measure mode, starts the measurement when the signal connected to the external gate input goes from high to low (falling edge); the measurement stops on the next falling edge of the gate signal.

- **Rising-edge external clock input** – In measure mode, starts or stops the measurement when the signal connected to the external C/T clock input pin goes from low to high (rising edge).

In continuous measure mode, starts the measurement when the signal connected to the external C/T clock input goes from low to high (rising edge); the measurement stops on the next rising edge of the C/T clock input signal.

- **Falling-edge external clock input** – Starts or stops a measure mode or continuous measure mode operation when the signal connected to the external C/T clock input pin goes from high to low (falling edge).

  In continuous measure mode, starts the measurement when the signal connected to the external C/T clock input goes from high to low (falling edge); the measurement stops on the next falling edge of the C/T clock input signal.

If you want to measure the frequency or period of a signal, specify the edges as one of the following:

- Start edge = rising; Stop edge = rising
- Start edge = falling; Stop edge = falling

In measure mode only, you can measure the pulse width of a signal by specifying the edges as one of the following:

- Start edge = rising; Stop edge = falling
- Start edge = falling; Stop edge = rising

Note: In measure mode and continuous measure mode, the internal C/T clock is used to calculate the interval of the signal between the specified start and stop edges. The pulse width and period count are automatically set to 0. In measure mode, you can specify the polarity of the output signal during and after the measurement.

Pulse Output Parameters

DT9840 Series modules can output pulses from each counter / timer. Table 4 lists the pin assignments of connector J17 on the module that correspond to the pulse output signals.

Table 4: Pulse Output Signals on the DT9840 Series Modules

Counter./Timer Pulse Output Signal	J17 Pin Number
Counter Output 0	5
Counter Output 1	3
Counter Output 2	1

You can specify the following pulse width parameters using software:

- Polarity, described below
- Period count, described on page 50
- Pulse width count, described on page 51

Polarity

You can specify one of the following values for the polarity of the pulse output signal:

- **Active high (low-to-high transitions)** – The high portion of the total pulse output period is the active portion of the counter / timer pulse output signal.
- **Active low (high-to-low transitions)** – The low portion of the total pulse output period is the active portion of the counter / timer clock output signal.

Period Count

By specifying the period count, you can determine the frequency of the pulse output signal.

Note: You can also use the period count in event counting operations to determine the value at which the counter / timer starts counting.

The period count defines the initial value that is loaded into the specified counter / timer. Values range from 1 to FFFFFFFFh. The counter / timer counts from the period count to FFFFFFFFh, rolls over to 0 (the terminal count), and then reloads the period count.

Use the following equations to determine the period count when performing pulse output operations:

- *PeriodCount* = FFFFFFFFh + 2 – (clock frequency / output frequency)

  For example, if the clock input frequency is 18 MHz and the desired pulse output frequency is 6.0 MHz, the required *PeriodCount* is FFFFFFFEh.

- #clks per output period = FFFFFFFFh + 2 – *PeriodCount*

  For example, if *PeriodCount* = FFFFFFFEh, three clocks occur for each output period. In this example, the counter counts FFFFFFFEh, FFFFFFFFh, 0, FFFFFFFEh, FFFFFFFFh, 0, and so on.

- output period = (# clks per output period) x (clock period)

  For example, if three clocks occur for each output period and the clock period is 55.555 ns, then the output period is 166.666 ns.

- output frequency = 1 / output period

  For example, if the output period is 166.666 ns, then the output frequency is 6.0 MHz

Pulse Width Count

The pulse width count determines when the output pulse of the counter / timer is activated. Values range from 1 to FFFFFFFFh.

Use the following equations to determine the value for the pulse width count:

- *PulseWidthCount* = FFFFFFFFh + 1 – (duty cycle x (clock frequency / output frequency))

  For example, if the clock input frequency is 18 MHz, the frequency of the output pulse is 6.0 MHz, and the desired duty cycle is .66 (66%), then the required *PulseWidthCount* is FFFFFFFEh.

- #clks per output pulse = FFFFFFFFh + 1 – *PulseWidthCount*

  For example, if *PulseWidthCount* = FFFFFFFEh, two clocks occur for each output pulse. In this example, the output is active for counts FFFFFFFFh and 0.

- output pulse width = (#clks per output pulse) x (clock period)

  For example, if the clock period is 55.55 ns and two clock occur for each output pulse, then the output pulse width is 111.11 ns.

- output duty cycle = (output pulse width) / (output period)

  For example, if the output pulse width is 222.2 ns and the output pulse period is 333.3 ns, then the output duty cycle is .66 (66%).

Counter/Timer Operation Modes

DT9840 Series modules support the following counter / timer operation modes:

- Standard counting (this includes event counting and rate generation)
- Measure

- Continuous measure
- Up / down counting
- One-shot
- Repetitive one-shot

You specify the mode using software. The following subsections describe these modes in more detail.

Standard Counting

Specify standard counting if you want to use the counter / timer to count events or generate a rate based on a count.

In event counting applications, the counter / timer counts pulses from an external C / T clock when the enabled gate signal (software, external normal, or external inverted) is active. Refer to page 43 for more information on the external C / T clock source; refer to page 45 for more information on gate types.

Since each counter / timer is 32 bits, you can count from 1 to FFFFFFFFh events before the counter rolls over to 0 and starts counting again. You can read the value of the counter at any time.

Using the period count, described on page 50, you can specify the initial count that is loaded into the counter / timer; the counter / timer starts counting from this value. Using the pulse width count, described on page 51, you can specify the count at which the counter / timer stops counting; when the counter reaches this value, a pulse is output from the counter / timer. You can specify the polarity of this output pulse, as described on page 49.

Figure 5 shows an example of an event counting operation using an normal external gate type.

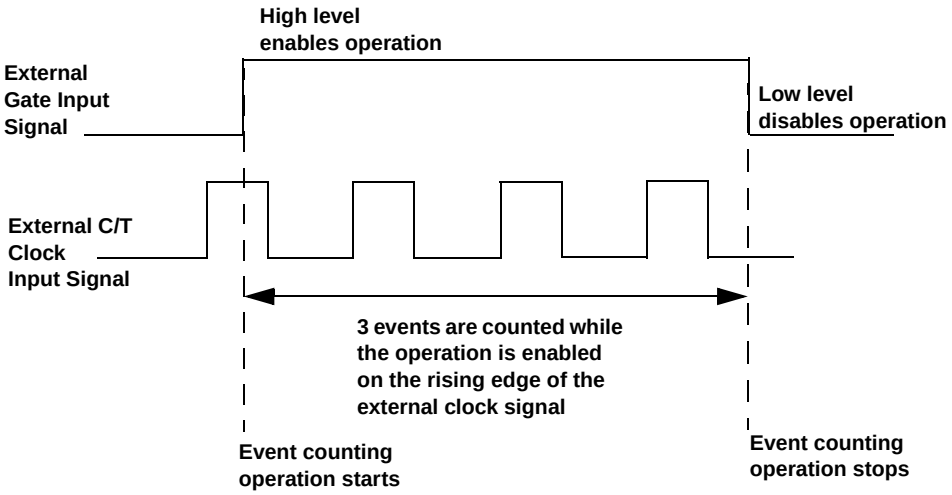


Figure 5: Example of Event Counting

In rate generation applications, a pulse output signal is output from the counter continuously; this mode is sometimes referred to as continuous pulse output or pulse train output. You can use this pulse output signal as an external clock to pace other operations, such as analog input or other counter/timer operations.

The internal C/T clock source starts the rate generation operation when the enabled gate signal (software, external normal, or external inverted) is active. Refer to page 43 for more information on C/T clock sources; refer to page 45 for more information on gate types.

You can specify the polarity of the output signal, the frequency of the pulse output signal using the period count, and the duty cycle of the pulse output signal using the pulse width count. Refer to page 49 for more information on the pulse output parameters.

The pulse output is activated when the counter increments to the pulse width count. The pulse output stays active until the counter rolls over to 0 (the terminal count). The pulse output is then deactivated and the counter is automatically reloaded with the period count. This sequence is repeated as long as the counter is enabled by the gate.

Figure 6 shows an example of a rate generation operation using an internal C/T clock source, normal gate type, period count of FFFFFFFEh, a low-to-high output pulse polarity, and a pulse width count of FFFFFFFEh to achieve a duty cycle of 66%. A 6.0 MHz square wave is the generated output.

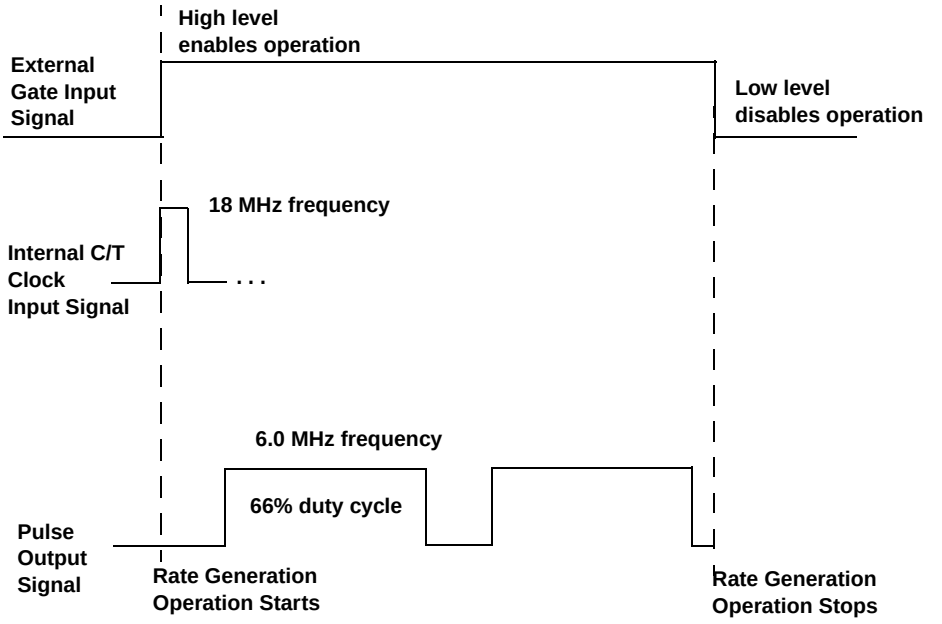


Figure 6: Example of Rate Generation Mode

Measure

Use measure mode to measure the interval between a selected start edge and a selected stop edge of a signal connected to the external C/T input pin or external gate input pin of the counter/timer. Refer to page 47 for more information on edge types and how to use them to measure frequency, period, and pulse width.

When you trigger the counter/timer in software, the counter increments from the time it detects the selected start edge until it detects the stop edge. When it detects the selected stop edge, the counter stops counting.

You can determine whether the measure mode operation is complete or not using software. When the operation is complete, you can read the value of the counter.

Use the following equations to determine the frequency, period, and pulse width of the signal:

- Frequency = 18 MHz/Number of Counts
- Period = 1/Frequency
- Pulse width = Number of Counts/18 MHz

Note: In measure mode, the internal C/T clock is used to calculate the interval of the signal between the specified start and stop edges. The pulse width and period count are automatically set to 0. You can specify the polarity of the output signal during and after the measurement.

Figure 7 shows an example of how to measure the pulse width of a signal. Ensure that the signals are wired appropriately. Refer to the *DT9840 Series Getting Started Manual* for wiring examples.

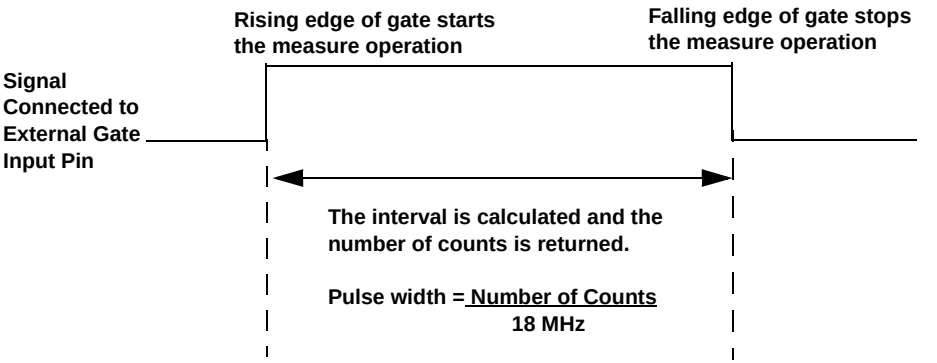


Figure 7: Example of Frequency Measurement

Continuous Measure

Use continuous measure mode to measure the interval between a selected start edge and the next start edge of a signal connected to the external C/T input pin or external gate input pin of the counter/timer. Refer to page 47 for more information on edge types and how to use them to measure frequency and period.

When it detects the specified start edge, the counter begins incrementing. The counter stops incrementing when it detects the next start edge. The stop edge is ignored.

When the operation completes, the counter remains idle until it is read. On the next read, the current value of the counter (from the previous measurement) is returned and the next measurement is started automatically.

Note: If you read the counter before the measurement is complete, 0 is returned.

For example, you might see results similar to the following if you read the counter / timer channel as part of the data stream:

Time	A/D Value	Counter/ Timer Value	Status of Continuous Measure Mode Operation
10	5002	0	Operation started when the C/T subsystem was configured, but is not complete
20	5004	0	Operation not complete
30	5003	0	Operation not complete
40	5002	12373	Operation complete
50	5000	0	Next operation started, but is not complete
60	5002	0	Operation not complete
70	5004	0	Operation not complete
80	5003	12403	Operation complete
90	5002	0	Next operation started, but is not complete

Use the following equations to determine the frequency and period of the signal:

- Frequency = 18 MHz / Number of Counts
- Period = 1 / Frequency

Note: In continuous measure mode, the internal C/T clock is used to calculate the interval of the signal between the first start edge and the next start edge. The pulse width and period count are automatically set to 0.

Figure 7 shows an example of how to measure the frequency of a signal. Ensure that the signals are wired appropriately. Refer to the *DT9840 Series Getting Started Manual* for wiring examples.

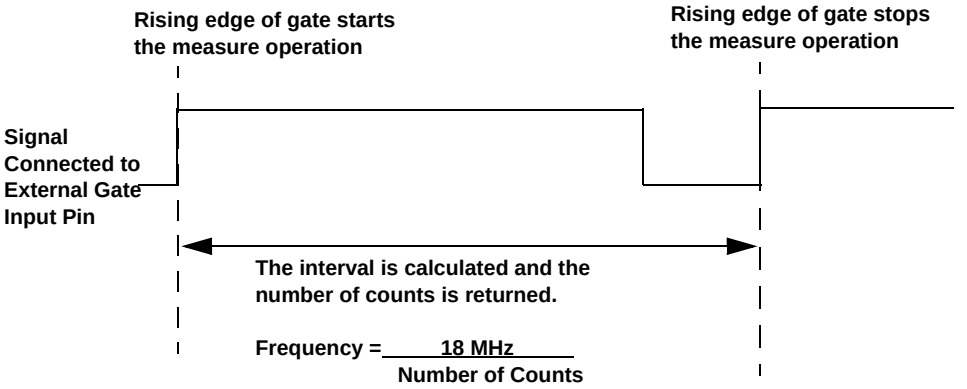


Figure 8: Example of Continuous Measure Mode - Measuring the Frequency

Up/Down Counting

Use up / down counting mode if you want to increment the counter when the specified external gate signal is enabled and decrement the counter when the specified external gate signal is disabled. This mode is useful when monitoring the position of an object, such as a lift on a shaker table, that can move in two directions.

When using a normal gate type, the counter / timer is incremented when the gate signal is high and decremented when the gate signal is low. If you are using an inverted gate signal, the counter / timer is incremented when the gate signal is low and decremented when the gate signal is high.

Note: This mode should be used only when the position of the object being monitored stays within the range of the counter, since the operation is not be reliable if the counter increments above FFFFFFFh or decrements below 0.

You can read the value of the counter at any time using software.

To use this mode, specify an external C / T clock source and either a normal or inverted external gate type. Refer to page 43 for more information on the external C / T clock source; refer to page 45 for more information on gate types.

Figure 5 shows an example of an up / down counting operation. Ensure that the signals are wired appropriately. Refer to the *DT9840 Series Getting Started Manual* for wiring examples.

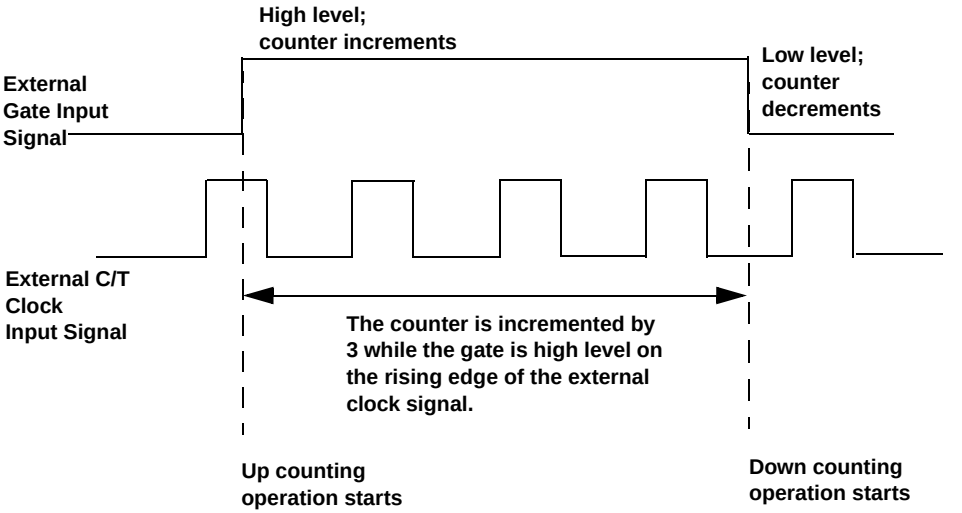


Figure 9: Example of Up/Down Counting

One-Shot

Use one-shot mode to generate a single pulse output signal from the counter when the operation is enabled by a either an external normal or inverted gate type. Refer to page 45 for more information on gate types. You can use this pulse output signal as an external digital (TTL) trigger to start other operations, such as an analog input operation.

When the operation is enabled, the counter begins incrementing. When the counter increments to the pulse width count, described on page 51, the value of the counter is output. The output stays active until the counter rolls over to 0 (the terminal count).

When the counter reaches the terminal count, the output is deactivated and the counter is automatically reloaded with the period count, described on page 50. The pulse output then stays inactive, and the counter stays disabled. All subsequent clock and gate signals are ignored.

You can specify the polarity of the output signal; refer to page 49 for more information.

In one-shot mode, the internal C/T clock source is more useful than an external C/T clock source. Refer to page 43 for more information on the internal C/T clock source.

Note: In the case of a one-shot operation, use a duty cycle as close to 100% as possible to output a pulse immediately. Using a duty cycle closer to 0% acts as a pulse output delay.

Figure 10 shows an example of a one-shot operation using an external normal gate signal, a period count FFFFFFFEh, a low-to-high output pulse polarity, and a pulse width count of FFFFFFFEh to achieve a duty cycle of 66%.

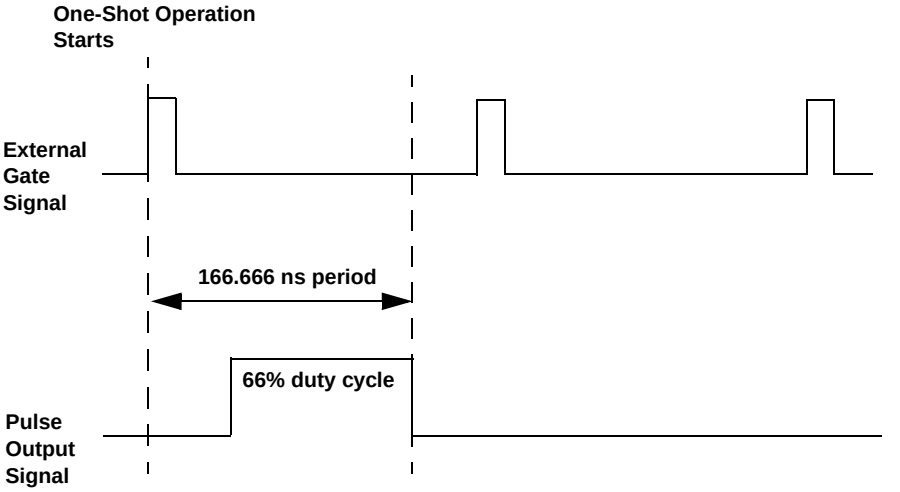


Figure 10: Example of One-Shot Mode

Repetitive One-Shot

Use repetitive one-shot mode to clean up a poor clock input signal by changing its pulse width, and then outputting it.

If you specify an external normal or inverted gate type, a single pulse is output each time the gate signal is active. For example, you could set up the counter to output a single pulse each time the gate signal changed from a high to low state. Refer to page 45 for more information on gate types.

When the operation is enabled with an external gate, the counter begins incrementing. When the counter increments to the pulse width count, described on page 51, the value of the counter is output. The output stays active until the counter rolls over to 0 (the terminal count). The output is then deactivated and the counter is automatically reloaded with the period count, described on page 50. The output then stays inactive, and the counter stays disabled, until the operation is re-enabled with the proper gate signal. All gate signals that occur while the counter is incrementing are ignored.

You can specify the polarity of the output signal; refer to page 49 for more information.

In repetitive one-shot mode, the internal C/T clock source is more useful than an external C/T clock source; refer to page 43 for more information on the internal C/T clock source.

Figure 11 shows an example of a repetitive one-shot operation using an external normal gate; a period count of FFFFFFFEh, a low-to-high output pulse polarity, and a pulse width count of FFFFFFFEh to achieve a duty cycle of 66%.

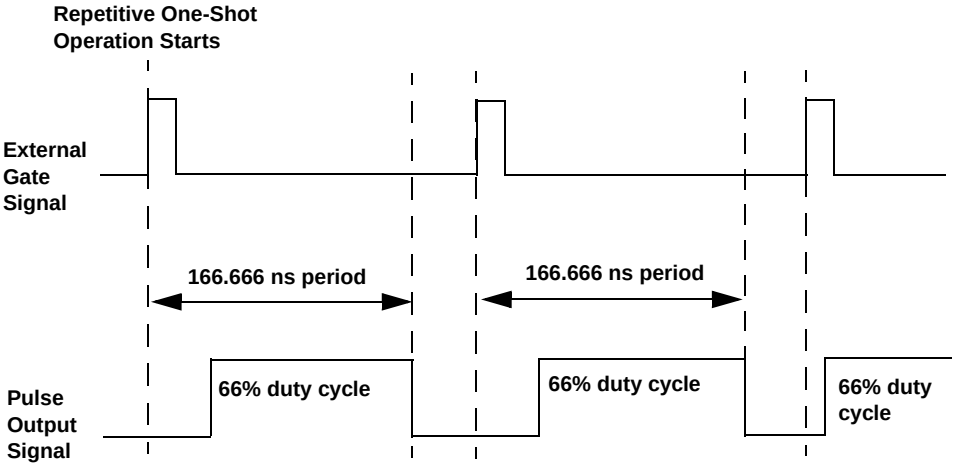


Figure 11: Example of Repetitive One-Shot Mode

2

Register Description

This section describes the registers that are used to program the DT9840 Series modules. Note that the following designations are used for the register types:

- R = Read
- W = Write
- R/W = Read and Write

All addresses discussed are in hexadecimal notation.

USB Bus/DSP Hardware Interface

Communication between the USB and DSP through the isolation barrier uses the 16-bit host port interface of the Texas Instruments TMS320C6713 DSP processor. (Note that a 100 ns delay is required to pass data through the isolators.) Refer to the *DT9840 Series DSP Library Reference Manual* for more information on programming the DSP.

The Hardware Control and Status register, described in Table 5, is located at address 0xB0000000.

Table 5: Hardware Control and Status Register (Address 0xB0000000)

Bit	Register Description	Value[a]	Type
0	Indicates whether power is ok.	1 = All power supplies are correct. 0 = Power supplies are not correct.	R/W
1	Indicates whether the USB cable was connected/disconnected.	1 = USB cable is connected/ disconnected; EXT_INT4 is asserted. Set this bit to 0 to clear it. (See also bit 17 of the Calibration register.) 0 = USB cable was not connected/disconnected.	R/W
2	Indicates whether a low-to-high transition was detected on the external trigger line.	1 = A low-to-high transition was detected on the External Trigger BNC. To clear this bit, set this bit or bit 29 to 0. 0 = No external trigger occurred.	R/W

Table 5: Hardware Control and Status Register (Address 0xB0000000) (cont.)

Bit	Register Description	Value[a]	Type
3	For the DT9841, DT9841E, and DT9841-VIB, indicates whether turbo mode is selected for the A/D and D/A subsystems. For the DT9842/2 and DT9842/8, this bit is reserved.	1 = Enables turbo mode for the A/D and D/A subsystems. The maximum clock rate is the same at 51.2 MHz for 200 kHz throughput. The accuracy degrades to 12-bits above 0.5 Nyquist.[b] 0 = Disables turbo mode.	R/W
4[c]	Indicates whether the green switch of LED CR1 (or CR6 on the DT9841E) is lit.	1 = Turn on the green switch of LED CR1 (or CR6 on the DT9841E). 0 = Turn off the green switch of LED CR1 (or CR6 on the DT9841E).	R/W
5[c]	Indicates whether the red switch of LED CR1 (or CR6 on the DT9841E) is lit.	1 = Turn on the red switch of LED CR1 (or CR6 on the DT9841E). 0 = Turn off the red switch of LED CR1 (or CR6 on the DT9841E).	R/W
6	Indicates whether EXT_INT4 is enabled if counter/timer 2 overflows/underflows.	1 = Enables EXT_INT4 if counter/timer 2 overflows/ underflows. 0 = Disables EXT_INT4 if counter/timer 2 overflows/ underflows.	R/W
7	Indicates whether counter/timer 2 has overflowed/underflowed in up/down counting mode.	1 = Counter/timer 2 has overflowed/ underflowed in up/down mode. This bit must be cleared (set to 0) by the DSP. 0 = Counter/timer 2 has not overflowed/underflowed in up/down mode.	R/W

Table 5: Hardware Control and Status Register (Address 0xB0000000) (cont.)

Bit	Register Description	Value[a]	Type
8	Indicates whether EXT_INT4 is enabled if counter/timer 1 overflows/underflows.	1 = Enables EXT_INT4 if counter/timer 1 overflows/ underflows. 0 = Disables EXT_INT4 if counter/timer 1 overflows/ underflows.	R/W
9	Indicates whether counter/timer 1 has overflowed/underflowed in up/down counting mode.	1 = Counter/timer 1 has overflowed/ underflowed in up/down mode. This bit must be cleared (set to 0) by the DSP. 0 = Counter/timer 1 has not overflowed/underflowed in up/down mode.	R/W
10	Indicates whether EXT_INT4 is enabled if counter/timer 0 overflows/underflows.	1 = Enables EXT_INT4 if counter/timer 0 overflows/ underflows. 0 = Disables EXT_INT4 if counter/timer 0 overflows/ underflows.	R/W
11	Indicates whether counter/timer 0 has overflowed/underflowed in up/down counting mode.	1 = Counter/timer 0 has overflowed/ underflowed in up/down mode. This bit must be cleared (set to 0) by the DSP. 0 = Counter/timer 0 has not overflowed/underflowed in up/down mode.	R/W
12	Indicates whether the Scalable Bus has been addressed or unaddressed.	1 = Scalable Bus has been addressed or unaddressed; EXT_INT4 is asserted. 0 = No Scalable Bus activity.	R

Table 5: Hardware Control and Status Register (Address 0xB0000000) (cont.)

Bit	Register Description	Value[a]	Type
13	Indicates whether the digital port 0 changed state.	1 = The data of digital port 0 has changed. 0 = The data of digital port 0 has not changed.	R
14	Indicates whether interrupt EXT_INT4 is asserted by the external trigger.	1 = Enables the external trigger to assert EXT_INT4. 0 = Disables the assertion of EXT_INT4 by the external trigger.	R/W
15	Reserved	0	R
16	Indicates whether to reset the A/D and D/A subsystems.	1 = Normal operation. 0 = Resets the A/D and D/A. The A/D and D/A should be reset each time the sample clock is changed.	R/W
17	Indicates whether digital port 2 is enabled for input or output.	1 = Port 2 is an output port. 0 = Port 2 is an input port.	R/W
18	Indicates whether digital port 1 is enabled for input or output.	1 = Port 1 is an output port. 0 = Port 1 is an input port.	R/W
19	Indicates whether digital 0 is enabled for input or output.	1 = Port 0 is an output port. 0 = Port 0 is an input port.	R/W
20	Indicates whether a deglitch function is used on digital port 0.	1 = Enables a 10 ms deglitch function on digital port 0. 0 = Disables the 10 ms deglitch function on digital port 0.	R/W
21	Indicates whether Digital Port 0 is enabled for EXT_INT4.	1 = Enables the interrupt-on-change function for EXT_INT4. 0 = Disables the interrupt-on-change function for EXT_INT4.	R/W

Table 5: Hardware Control and Status Register (Address 0xB0000000) (cont.)

Bit	Register Description	Value[a]	Type
22, 23	For the DT9841, DT9841E, and DT9841-VIB, indicates whether D/A filters or 0 V outputs are used. For the DT9842/2 and DT9842/8, these bits are reserved.	Bit 23 Bit 22 0 0 = Switches ON the 4-pole, 5 kHz filters for both D/A outputs 0 1 = Switches ON the 4-pole, 20 kHz filters for both D/A outputs. 1 0 = Passes the D/A data out without filtering. 1 1 = Sends 0 V out.	R/W
24	Indicates that the D/A data is ready (D/A Write clears).	1 = D/A ready for new data. Data is clocked out of the data register. This bit is cleared (set to 0) automatically when new D/A data is loaded into the data register. 0 = D/A converting data.	R
25[d]	Indicates whether a D/A underrun error occurred.	1 = New data has not been loaded into the two D/A data registers before the next clock pulse; interrupt EXT_INT4 is asserted. This bit must be cleared by the DSP or the host. Conversions do not stop; however, the data may be corrupt. 0 = New data has been loaded into the two D/A data registers before the next sample clock; no error.	R/W

Table 5: Hardware Control and Status Register (Address 0xB0000000) (cont.)

Bit	Register Description	Value[a]	Type
26	Indicates whether the A/D conversion is done (A/D Read clears).	1 = A/D converters are finished converting the data. This bit is cleared (set to 0) automatically when the DSP reads the data. This bit asserts EXT_INT6. 0 = A/D conversions are not finished.	R/W
27[e]	Indicates whether an A/D overrun error occurred.	1 = A/D data was not read before the next conversion was completed; interrupt EXT_INT4 is asserted. This bit must be cleared (set to 0) by the DSP or host. Conversions do not stop; however, the data may be corrupt. 0 = A/D data was read before the next conversion was completed; no error.	R/W
28	Indicates whether A/D and D/A interrupts are enabled. This bit is controlled by the DSP.	1 = Enables A/D and D/A interrupts. 0 = Disables A/D and D/A interrupts.	R/W
29	Indicates whether an external trigger is used. This bit is controlled by the DSP.	1 = A/D and D/A conversion process starts on the low-to-high transition on the Ext Trigger BNC. 0 = Software trigger is used.	R/W

Table 5: Hardware Control and Status Register (Address 0xB0000000) (cont.)

Bit	Register Description	Value[a]	Type
30	Indicates that an external clock is used. This bit is controlled by the DSP.	1 = A/D and D/A clock must be provided on the Ext Clock BNC. This bit must be set to 1 on any slave modules. For the DT9841, DT9841E, and DT9841-VIB, the frequency of of the external clock source that is used must be 256 times the required sampling frequency. (For example, if the required sampling frequency is 100 kHz, use an external clock source with a frequency of 25.6 MHz.) 0 = The internal clock is used.	R/W
31	Indicates where the clock and trigger signals come from. This bit is controlled by the DSP.	1 = The module receives all A/D and D/A clocks and triggers from the scalable bus. The internal DSP and counter/timers operate on their own independent clock. This setting is used for slave modules. 0 = The module receives all A/D and D/A clocks and triggers from its own inputs (not from the scalable bus). This setting is typically used by the master module only.	R/W

a. All bits power up in the "0" state. When all the power supplies are correct, bit 0 switches to "1," indicating the module is ready for use.

b. This mode is currently not supported in software.

c. A two-color LED (CR6 on the DT9841E module, CR1 on all other modules) is visible from the back of the module. When power is applied to the module, this LED turns green. When the module is recognized by the host and the firmware is downloaded to the module, the LED turns red. When the Windows driver is loaded and started, the LED turns orange.When you download and run your DSP program, this LED flashes green and orange. When you download and run your DSP program, this LED flashes green and orange. If the downloaded program stops running, this LED turns stops flashing (in either the green or orange state) to indicate that an error occurred, and the debug LEDs (CR7 to CR14) turn on. You can define the state of the debug LEDs using software. Four address LEDs (CR15) indicate the Scalable Bus address; position M is the master and positions 1, 2, and 4 are turned on as needed to represent the slave address. The intensity of the LEDs for the addressed module is brighter than the LEDs for the nonaddressed modules. Debug and Address LEDs are not supported on the DT9841E.
d. This bit is set if the data in the input latch has not been updated on the next D / A clock. At the fastest clock rate, this means that the data must be updated within 10 µs.
e. This bit will be set if the A / D clock is faster than the A / D converter specification or if the data was not read fast enough by the DSP or host.

Calibration and Setup

The Calibration and Setup register, described in Table 6, is located at address 0xB0000004. Address 0xB0000001 is the control register for the Xicor potentiometers, bias return resistors, and Scalable Bus termination resistors. The register select is CE3, described in Table 15 on page 110, and requires a clock divider of four (40 ns).

Table 6: Calibration and Setup Register (Address 0xB0000004)

Bit	Register Description[a]	Type
0 to 13	Reserved	R
14	When 1, sets the module for IEPE operation; streaming writes to DIO port 2 are disabled. When 0, sets the module for normal operation; streaming writes to DIO port 2 are enabled.	R/W
15	For the DT9841, DT9841E, and DT9841-VIB when 1, sets the DAC voltage range to ±2.5 V; when 0, sets the DAC voltage range to ±10 V. For the DT9842/2 and DT9842/8, this bit is reserved. The DAC voltage range is always ±10 V.	R/W
16	When 1, enables writing to the digital ports under DMA mode; when 0, disables writing to the digital ports under DMA mode.	R/W
17	When 1, the USB cable is connected; when 0, the USB cable is not connected.	R
18	DSP heartbeat signal readable by the USB interface without having to go through the host port interface. This bit is toggled by the DSP program to indicate the program is running.	R/W

Table 6: Calibration and Setup Register (Address 0xB0000004) (cont.)

Bit	Register Description[a]	Type
19	Data input bit for the Xicor potentiometer (see also bit 31).	R
20	When 1, enables the chip that controls the A/D 1 kΩ termination resistors (see bits 26 and 27). When 0, disables the chip that controls the A/D termination resistors.	R/W
21	For the DT9841, DT9841E, and DT9841-VIB, data from the D/A (MDO line). For the DT9842/2 and DT9842/8, this bit is reserved.	R/W
22	For the DT9841, DT9841E, and DT9841-VIB, data to the D/A (MDI line). For the DT9842/2 and DT9842/8, this bit is reserved.	R/W
23	For the DT9841, DT9841E, and DT9841-VIB, clock for the D/A (MC line). For the DT9842/2 and DT9842/8, this bit is reserved.	R/W
24	For the DT9841, DT9841E, and DT9841-VIB, select for the D/A (ML line). For the DT9842/2 and DT9842/8, this bit is reserved.	R/W
25	When 1, enables the Scalable Bus 100 Ω termination resistors; write to address 0xB000000C. When 0, disables the Scalable Bus 100 Ω termination resistors.	R/W
26[b]	Data bit for the chip that controls the 1 kΩ termination resistors on the A/D inputs (see bits 20 and 27).	R/W
27[b]	Serial clock for the chip that controls the 1 kΩ termination resistors on the A/D inputs (see bits 20 and 26).	R/W
28[c]	Data bit for the programmable clock chip (CY data).	R/W

Table 6: Calibration and Setup Register (Address 0xB0000004) (cont.)

Bit	Register Description[a]	Type
29[c]	Clocks the serial port of the CY clock (address 69h).	R/W
30	Data output bit for the Xicor potentiometers (see bit 31). When 1, the pin is in tristate so that the data can be read at bit 19; write to address 0xB000000C.	R/W
31	Clocks the serial port of the Xicor (Xicor X9258WS) potentiometers that are used for calibrating the zero and full scale values of the A/Ds and D/As; write to address 0xB000000C.	R/W

a. All bits power up in the "0" state. Typically, these bits are controlled from the host through the host port interface.

b. Bits 26 and 27 control the termination multiplexer. In differential mode, any or all of the analog input Lo signals can be terminated with the 1 kΩbias return resistor to the isolated analog common. The termination function can be initiated independently from all other functions.

c. On the DT9841, DT9841E, and DT9841-VIB, the frequency of the MCLK signal is multiplied by 512, and then divided by 2; the base frequency is 36.00 MHz. For example, if you specify a frequency of 100 kHz for the internal sample clock, the MCLK signal (100 kHz) is multiplied by 512 (51.2 MHz), and then divided by two (25.6 MHz), synchronized to the CAL command of the serial input, and buffered for output in the Spartan chip. After the A/D reset is released, valid data is available in 1116 * 1/sample rate (or 11.16 ms at 100 kHz). Refer to the documentation for CY22150 for programming information; the address of CY22150 is 0x69h (3 ms settling time required for the DLL).

The module has Xicor X9258US24-2.7 EE potentiometers to support software calibration of the A/D subsystem. All calibration is done in differential mode with all channels connected together and to analog common. Data is continuously acquired at 50 kHz; the results of the averaged conversions are printed to the display. A low noise, programmable voltage source similar to Electronic Development Corporation's Model 501J should be used to calibrate the A/D subsystem.

The following sections describe the calibration process.

Setting Up the Xicor Potentiometers

Control I/O line SDA is provided for serial data and SCL is provided for the serial clock. All commands are preceded by a high to low transition on SDA while SCL is high. All communication must be terminated with a low to high transition on SDA while SCL is high. SCL must be high and low for 5 µs minimum (100 kHz).

Rather than push the high and low timing in a Windows environment, it is suggested that a 10 µs high and low period be established, with the data transitions taking place in the center (50 kHz). Slowing the timing down further will not cause any errors.

Note: ACK (Acknowledge) and Read Back are not be available on the DT9841, DT9841E, and DT9841-VIB module. To calibrate the module, the potentiometer must be reset by writing the lowest value, and then incrementing it until the correct value is set.

After each byte of data is transferred, an ACK low-going signal can be read on the SDA line on the 9th high-going, low SCL signal. The data is valid 4.7 µs after the SCL switches from low to high and 0.3 µs after the high-to-low transition.

The first byte sent after a start command must be the device type followed by the address. The device type is 0101 for a X9258; the addresses for the potentiometers are listed in Table 7.

Table 7: Xicor Potentiometer Addresses and Functions

Address	Potentiometer	Function
0000	0	A/D 0 Zero Calibration
0000	1	A/D 1 Zero Calibration
0000	2	A/D 2 Zero Calibration
0000	3	A/D 3 Zero Calibration
0001	0	A/D 4 Zero Calibration
0001	1	A/D 5 Zero Calibration
0001	2	A/D 6 Zero Calibration
0001	3	A/D 7 Zero Calibration
0010	0	A/D 0 Full Scale Calibration
0010	1	A/D 1 Full Scale Calibration
0010	2	A/D 2 Full Scale Calibration
0010	3	A/D 3 Full Scale Calibration
0011	0	A/D 4 Full Scale Calibration
0011	1	A/D 5 Full Scale Calibration
0011	2	A/D 6 Full Scale Calibration
0011	3	A/D 7 Full Scale Calibration
0100	0	D/A 0 Zero Calibration
0100	1	D/A 1 Zero Calibration
0100	2	D/A 0 Full Scale Calibration
0100	3	D/A 1 Full Scale Calibration

Table 8 describes the instruction set for the Xicor potentiometers.

Table 8: Xicor Potentiometer Instruction Set

Instruction	Instruction Format								Operation
	I3	I2	I1	I0	P1	P0	R1	R0	
Read WCR	1	0	0	1	1/0	1/0	N/A	N/A	Read the contents of the wiper counter register pointed to by P1-P0.
Write WCR	1	0	1	0	1/0	1/0	N/A	N/A	Write new value to the wiper counter register pointed to by P1-P0.
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the register pointed to by P1-P0 and R1-R0.
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the register pointed to by P1-P0 and R1-R0.
XFR Data Reg to WCR	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the register pointed to by P1-P0 and R1-R0 to its associated WCR.
XFR WCR to Data Reg	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the WCR pointed to by P1-P0 to the register pointed to by R1-R0.

Table 8: Xicor Potentiometer Instruction Set (cont.)

Instruction	Instruction Format								Operation
	I3	I2	I1	I0	P1	P0	R1	R0	
Global XFR Data to WCR	1	0	0	1	N/A	N/A	1/0	1/0	Transfer the contents of all four Data Registers pointed to by R1-R0 to their respective WCR.
Global XFR WCR to Data	1	0	0	0	N/A	N/A	1/0	1/0	Transfer the contents of all WCRs to their respective data registers pointed to by R1-R0.
Inc / Dec Wiper	1	0	1	0	1/0	1/0	N/A	N/A	Enable increments/decrements of the WCR pointed to by P1-P0.

Calibrating the Analog Input Subsystem

Note: For simultaneous sample-and-hold applications, the rising edge of the CAL signal must be timed with the falling edge of the MCLK signal.

In bipolar mode with 24-bit or 16-bit converters, after each WCR write, a 500 µs delay must be implemented to allow the wiper to settle before reading the next A / D conversion. The wiper must be incremented through the center value and then be backed off to center the A / D code on the proper code. Data must also be averaged for maximum reliability. It is suggested a minimum of 16 values be taken for the averaging routine.

To calibrate the A / D converters on the DT9841, DT9841E, and DT9841-VIB, do the following:

4. Set the A / D converters to 0 by applying 0.00000 volts on all channels and adjust the potentiometer on each A / D channel for a code of 00000000h. Refer to Table 7 on page 79 for the address of each potentiometer.
5. Set the full-scale range by applying +9.37500 V on each channel and adjust the potentiometer on each A / D channel for a code of 2013265664 or 77FFFF00h.

To calibrate the A / D converters on the DT9842 / 2 and DT9842 / 8, do the following:

1. Set the A / D converters to 0 by applying 0.00000 volts on all channels and adjust the potentiometer on each A / D channel for a code of 00000000h. Refer to Table 7 on page 79 for the address of each potentiometer.
2. Set the full-scale range by applying +9.37500 V on each channel and adjust the potentiometer on each A / D channel for a code of 63488 or F8000000h.

To store the A / D calibration, transfer the contents of P0 through P3 to their respective R0 through R3 registers. This is a nonvolatile write operation and require 10 ms before any other operation. When the module powers up, the values in the R0 locations are automatically moved to the WCR location, placing the calibration values on the outputs. The value stored in location R1 is the backup value for R0.

Calibrating the Analog Output Subsystem

To calibrate the DACs on the DT9841, DT9841E, and DT9841-VIB, do the following:

1. Set the DACs to 0 V by writing a code of 00000000h on both DACs.
2. Set the EEPOT by incrementing (to decrease the output) or decrementing (to increase the output) until the outputs equal 0.00000 V ±0.0004 V. Each step changes the output by 0.3 mV. There are a total of 256 steps. Refer to Table 7 on page 79 for the address of each potentiometer.
3. Set the full-scale by writing a code of 77FFFF00h on both DACs and adjusting the appropriate potentiometers for an output voltage of +9.37500 V.

To calibrate the DACs on the DT9842/2 and DT9842/8, do the following:

1. Set the DACs to -10 V by writing a code of 00000000h to both DACs.
2. Set the EEPOT by incrementing (to decrease the output) or decrementing (to increase the output) until the outputs equal -10.000 V ±0.0004 V. Each step changes the output by 0.3 mV. There are a total of 256 steps. Refer to Table 7 on page 79 for the address of each potentiometer.
3. Set the full-scale by writing a code of FFFF0000h on both DACs and adjusting the appropriate potentiometers for an output voltage of +9.999695 V. Refer to Table 7 on page 79 for the address of each potentiometer.

To store the D/A calibration, transfer the contents of P0 through P3 to their respective R0 through R3 registers. This is a nonvolatile write operation that requires 10 ms before any other operation. When the module powers up, the values in the R0 locations are automatically moved to the WCR location, placing the calibration values on the outputs. The value stored in location R1 is the backup value for R0.

Analog Input Subsystem

On the DT9841E, the A / D subsystem consists of two A / D converters that are simultaneously clocked. On all other DT9840 Series modules, the A / D subsystem consists of eight A / D converters that are simultaneously clocked.

On the DT9841, DT9841E and DT9841-VIB, the major components of this subsystem are the Delta-Sigma A / D converters and the sample clock oscillator. The Delta-Sigma converters remove anti-aliasing on the analog inputs and outputs. The sample clock (MCLK) determines the sampling rate at which all analog input channels, all digital input channels, and all counter / timer channels are simultaneously sampled. The minimum clock rate is 2 kSamples / s once the subsystems have been configured and started. For lower sampling rates, the DSP chip needs to be set up to discard unneeded samples using a filtering algorithm. The maximum clock rate is 100 kSamples / s. A digital filter is used to scale with the sampling rate.

On the DT9842 / 2 and DT9842 / 8, the major components of this subsystem are the successive approximation A / D converters and the sample clock oscillator. A 32-bit Clock Divider register (address 0xB0000008) controls the sampling rate of both the A / D and D / A converters. The value of this register divides the onboard 18 MHz sample clock oscillator. The default value of this register at system reset (and the maximum value that this register should be set to) is 180 (0xB4); this value results in a maximum sampling rate of 100 kSamples / s.

Using bit 30 of the Hardware and Control Status register, described in Table 5 on page 67, you can select either an internal or external clock source. MCLK is programmed using bits 28 and 29 of the Calibration and Setup register, described in Table 6 on page 75. When the external clock is selected, conversion begin on the high-to-low transition after a rising edge of the internal CAL signal.

On the DT9841 and DT9841E, any or all of the analog input low signals can be terminated with a 1 kΩ bias return resistor to the isolated analog common. Bits 20, 26, and 27 of the Calibration and Setup register, described in Table 6 on page 75, control the termination multiplexer. The termination function can be initiated independently from all other functions.

To initialize the A/D subsystem on the DT9841, DT9841E, or DT9841-VIB, serial port 0 (TI PCM1804) is used in SPI mode, and the A/Ds are set up for control port mode. Oversampling mode is 64x with a data width of 24 bits and twos complement data encoding; high-pass filtering is defeated. Note that this serial port is also used to synchronize up to seven additional slave modules, set up with an external clock. All connected modules receive the same setup information for the A/D and D/A subsystems over the Scalable Bus (see page 113 for more information on the Scalable Bus). Note that the rising edge of the CAL signal must be timed with the falling edge of the MCLK signal for simultaneous sample-and-hold operations. This is synchronized in the Spartan chip on the master module.

No initialization is required for the A/D subsystem on the DT9842/2 and DT9842/8 modules. The A/D converters are wired for the desired operation.

A/D conversions start on an internal (software) trigger or external trigger. An internal trigger is initiated by a software command. An external trigger is initiated by a low-to-high transition on the external TTL trigger input to the module; this trigger asserts EXT_INT4 for processing. Scanning is continuous through all A/D channels, digital inputs, and counter/timers. The DSP program can discard unneeded data.

On the DT9841, DT9841E, and DT9841-VIB, once the A/Ds are started, the serial data is packed as 32 bits in the Spartan chip. The data is left-hand justified (the right 8 bits are filled with zeros) and the data encoding is twos complement.

On the DT9842/2 and DT9842/8, once the A/Ds are started, the data is packed as 32 bits in the Spartan chip and the data is left-hand justified (the right 16 bits are filled with zeros, the data encoding is twos complement).

Interrupt EXT_INT6 is asserted to the DSP chip when the conversion is completed (A/D Done) and the data is ready (INT6 = pin D2). This interrupt initiates a DMA transfer on DMA channel 6. The acquired data is stored in the input FIFO and either sent to the DSP for further processing or to host memory over the USB bus. All samples must be read before the next A/D Done.

An orderly stop is done when the DSP firmware stops sending data to the host, but leaves the A/D running, discarding new data. This allows the module to transfer the last sample to the host or memory and restart data collection without performing another calibration.

The A/D error bit (bit 27 of the Hardware Control and Status register, described in Table 5 on page 67) is set if the A/D clock is set faster than the A/D converter specification or if the data was not read fast enough by the DSP or host. This error must be cleared by the DSP or host.

Table 9 describes the DMA address map.

Table 9: DMA Address Map

Address	Register Description	Type
0xB0004000	A/D Data 0 above physical memory, read only	R
0xB0004004	A/D Data 1	R
0xB0004008	A/D Data 2[a]	R
0xB000400C	A/D Data 3[a]	R
0xB0004010	A/D Data 4[a]	R

Table 9: DMA Address Map (cont.)

Address	Register Description	Type
0xB0004014	A/D Data 5[a]	R
0xB0004018	A/D Data 6[a]	R
0xB000401C	A/D Data 7[a]	R
0xB0004020	Flag Bits, Digital Port 2[b], Digital Port 1, Digital Port 0[c]	R
0xB0004024	Counter Timer 0	R
0xB0004028	Counter Timer 1	R
0xB000402C	Counter Timer 2	R

a. Ignore the data in this register for DT9841E modules.
b. For the DT9841-VIB module, bit 0 of digital port 2 is used as the SCL clock and bit 1 of digital port 2 is used as the SDA data output; the remaining bits (2-7) of digital port 2 are reserved. See page 75 for more information.
c. Note that the digital ports are located at address 0xB0004020 along with the flag bits. This allows a single burst through the sequential addresses to acquire all the input data and flags. (Active state = 1). All reads are done at the 40.0 ns clock rate using the CE3 setup. Refer to Table 10 for more information on the flag bits. Refer to Table 15 on page 110 for more information on CE3.

Table 10 describes the flags at address 0xB0004020.

Table 10: Flags at Address 0xB0004020

Bit	Register Description
24	1 = Temperature is 65° C or over. 0 = Temperature is under 65° C.
25	1 = Counter/timer 2 has overflowed (this is the same as bit 7 of the Control and Status register). 0 = Counter/timer 2 has not overflowed.
26	1 = Counter/timer 1 has overflowed (this is the same as bit 9 of the Control and Status register). 0 = Counter/timer 1 has not overflowed.
27	1 = Counter/timer 0 has overflowed (this is the same as bit 11 of the Control and Status register). 0 = Counter/timer 0 has not overflowed.
28	1 = A FIFO Full /Error occurred on the Scalable Bus. 0 = A FIFO Full /Error did not occur on the Scalable Bus.
29	1 = A D/A trigger occurred. 0 = A D/A trigger did not occur.
30	1 = An A/D trigger error occurred. 0 = An A/D trigger error did not occur.
31	1 = An A/D trigger occurred. 0 = An A/D trigger did not occur.

Analog Output Subsystem

The DT9841, DT9841E, and DT9841-VIB support two 24-bit analog output channels. The major components of the analog output subsystem are the DACs, parallel to serial shifter, and the 20 kHz and 5 kHz output filters.

The DT9842/2 supports two 16-bit analog output channels and the DT9842/8 supports eight 16-bit analog output channels. The major components of the analog output subsystem are the DACs (no filtering is supported).

The clock and trigger are the same as the analog input subsystem, described on page 85.

Updating the DACs is a multistep process. The DSP must first write a value to the Spartan chip; the Spartan chip then performs a parallel to serial conversion, shifting the clocked data out to the appropriate DAC.

The digital data is double buffered within each DAC to prevent spurious outputs. Data in the second register stage of the DAC is output as an analog signal. Upon power up, both DACs are initialized to 0 V by the hardware. Note that a system reset does not change the value in either register stage of the DACs.

To initialize the D/A subsystem on the DT9841, DT9841E, and DT9841-VIB, serial port 0 (TI PCM1737) is used to set up the DACs and to synchronize up to seven additional modules. The added modules must be set up as slaves with an external clock. All connected modules receive the same setup information for the A/D and D/A subsystems over the Scalable Bus (see page 113 for more information on the Scalable Bus.) The serial port is also used to reset and start the DACs. The default mode is 128 times the sampling rate, 0 dB attenuation, DACs enabled, mute disabled, sharp roll-off, deemphasis disabled, 8 times interpolation, and 24-bit standard

format. For clock rates over 100 kHz, the over-sampling rate is 64 times.

On the DT9842/2 and DT9842/8, a system reset is used to initialize the DACs. No other initialization is necessary; the DACs are wired for the desired operation.

Once the DACs are started, the serial data is packed as 32 bits in the Spartan chip; the data is encoded as twos complement and is left-hand justified. On the DT9841, DT9841E, and DT9841-VIB, the right eight bits are filled with zeros. On the DT9842/2 and DT9842/8, the data is converted to 16-bit offset binary in the Spartan chip.

After the data is clocked out, the D/A Ready register asserts interrupt EXT_INT5. Then, both DACs must be updated within 10 µs (for 100 kHz operation) using DMA channel 5.

On the DT9841, DT9841E, and DT9841-VIB, the D/A data must always be output as two 32-bit words (channel 0 then channel 1). The data is clocked into the internal serial output register on the second word address. The initial value must be the code for 0 V output to preventing glitching after power up.

On the DT9842/2 and DT9842/8, the D/A data is output only when the corresponding register in the Spartan chip is written.

Bits 23 and 22 of the Hardware and Control Status register, described in Table 5 on page 67, must be set to 1 on power up. The digital output address follows the D/A address so that it can be included in the DMA list.

Bit 25 of the Hardware and Control Status register described in Table 5 on page 67, is set if the data in the input latch has not been updated on the next D/A clock. This will be 10 µs at the fastest clock rate. The error bit must be cleared by the host.

Table 9 describes the D/A data address map.

Table 11: D/A Data Address Map

Address	Register Description	Type
0xB0008000	D/A Data 0 above physical memory.	W
0xB0008004	D/A Data 1 above physical memory.	W
0xB0008008	Reserved zeros, digital port 2[a], digital port 1, digital port 0	W

a. For the DT9841-VIB module, bit 0 of digital port 2 is used as the SCL clock and bit 1 of digital port 2 is used as the SDA data output; the remaining bits (2-7) of digital port 2 are reserved. See page 75 for more information.

Digital I/O Subsystem

The DT9841-VIB provide 16 digital I/O signals (ports 0 and 1). Bit 0 of digital port 2 is used as the SCL clock and bit 1 of digital port 2 is used as the SDA data output; the remaining bits (2-7) of digital port 2 are reserved. You must turn streaming writes to digital port 2 off; see page 75 for more information.

All other DT9840 Series modules provide 24 digital I/O signals (ports 0, 1, and 2). You can program each port for input or output using bits 17, 18, and 19 of the Hardware Control and Status register, described in Table 5 on page 67. As inputs, the data on the ports is sampled at 25 MHz.

To read all the digital ports at once, use register 0xB0004020. To write to all the digital ports at once, use register 0xB0008008. To read or write to digital port 0 only, use register 0xB0010004. To read or write to digital port 1 only, use register 0xB0010008. To read or write to digital port 2 only, use register 0xB001000C. Refer to Table 15 on page 110 for more information on these registers.

When port 0 is configured as an input port, you can program the mask register located at address 0xB0010000 to generate an interrupt when any bit of port 0 changes state. In this mode, the sample rate changes to 1 MHz. Refer to Table 15 on page 110 for more information on this register. To enable the interrupt, set bit 21 of the Hardware Control and Status register, described in Table 5 on page 67. The data is right justified, aligning with digital port 0.

Additionally, you can minimize false triggers due to noise on digital input port 0 by enabling a 10 ms deglitch function using bit 20 of the Hardware Control and Status register, described in Table 5 on page 67.

All digital inputs are +5 V tolerant. All digital outputs include diode protection to isolated ground and isolated +5 V. The outputs are disabled on power-up and remain in the previous state on USB reset.

Counter/Timer Subsystem

User counter / timers 0, 1, and 2 provide software-selectable clocks, gates, operation modes, and output parameters described in more detail from the register perspective in the following sections. This provides the capability to generate rates, generate one-shots, count events, and determine the signal pulse width, signal period, and the time between two signals.

Table 12 describes the counter / timer address map, Table 13 describes the User Control registers at addresses 0xB000C020, 0xB000C024, and 0xB000C028, and Table 14 describes the User Status register at address 0xB000C030.

Note: Counter / timer 3 is a future option, designated as counter 1 in the 6713 chip. It is 32-bits wide and the input is gated in software. This gate is double-pinned on top of bit of port 0 and the input is double-pinned on top of bit 1 of port 0.

Table 12: Counter/Timer Address Map

Address[a]	Register Description	Type
0xB000C000[b]	User Period Register 0/ Counter 0	R/W
0xB000C004[b]	User Period Register 1/ Counter 1	R/W
0xB000C008[b]	User Period Register 2/ Counter 2	R/W
0xB000C00C	Reserved	–
0xB000C010[c]	User Pulse Register 0	W
0xB000C014[c]	User Pulse Register 1	W
0xB000C018[c]	User Pulse Register 2	W

Table 12: Counter/Timer Address Map (cont.)

Address[a]	Register Description	Type
0xB000C01C	Reserved	–
0xB000C020[d]	User Control 0	W
0xB000C024[d]	User Control 1	W
0xB000C028[d]	User Control 2	W
0xB000C02C	Reserved	–
0xB000C030[e]	User Status	R

a. All registers require 4 bytes of address space.
b. Bits 31 to 0 are used to specify the period of the counter / timer. Data written to this location is stored in the period register, and then immediately loaded into the counter / timer. Reads of this location return the current value of the counter / timer. This register and counter / timer are set to 0 on power up or when the counter / timer is reset.
c. Bits 31 to 0 are used to specify when the output pulse of the user counter / timer is activated. Data written to this location is stored in the pulse register. This register and counter / timer are set to 0 on power up or when the counter / timer is reset.
d. See Table 13.
e. See Table 14 on page 100.

Table 13: User Control Registers
(Addresses 0xB000C020, 0xB000C024, 0xB000C028)

Bit	Register Description	Value	Type
1:0	User Clock Select [1:0] These bits specify the clock for the user counter/timer. These bits resets to 00 on power up or Counter/Timer reset.	Bit 1 Bit 0 0 0 = Internal 18 MHz Clock 0 1 = External Clock 1 0 = Cascaded Clock 1 1 = Reserved	W
3:2	User Gate Select [1:0] These bits specify the gate for the user counter. These bits reset to 00 on power up or Counter/Timer reset.	Bit 3 Bit 2 0 0 = Logic Low (disabled) 0 1 = Logic High (enabled) 1 0 = External Gate (high active) 1 1 = External Gate Inverted (low active)	W
5:4	User Mode Select [1:0] These bits specify the mode for the user counter. These bits reset to 00 on power up or Counter/Timer reset.	Bit 5 Bit4 0 0 = Non-retriggerable One-Shot 0 1 = Retriggerable One-Shot 1 0 = Continuous Increment 1 1 = Auxiliary (see aux mode select bits)	W
6	User Output Polarity This bit specifies the polarity for the user output. This bit resets to 0 on power up or Counter/Timer Reset.	0 = Low Active 1 = High Active	W

Table 13: User Control Registers (Addresses 0xB000C020, 0xB000C024, 0xB000C028) (cont.)

Bit	Register Description	Value	Type
7	User One-Shot Trigger Enable Command The host should set up all the features/characteristics of the counter before issuing this command.	0 = One-shot triggers disabled. 1 = One-shot triggers enabled.	W
9:8	User Aux Mode Select [1:0] These bits specify the auxiliary mode for the user counter/timer.They only matter if the mode select bits specify auxiliary mode. These bits reset to 00 on power up or Counter/Timer reset.	Bit 9 Bit8 0 0 = Measure 0 1 = Up/down 1 0 = Reserved 1 1 = Reserved	W
11:10	User Measure Start Select [1:0] These bits specify the edge that starts the measurement. These bits reset to 00 on power up or Counter/Timer reset.	Bit 11 Bit10 0 0 = Selected gate (external, external inverted, or software) rises 0 1 = Selected gate (external, external inverted or software) falls 1 0 = External clock rises 1 1 = External clock falls	W

Table 13: User Control Registers (Addresses 0xB000C020, 0xB000C024, 0xB000C028) (cont.)

Bit	Register Description	Value	Type
13:12	User Measure Stop Select [1:0] These bits specify the edge that stops the measurement. These bits reset to 00 on power up or Counter/Timer Reset.	Bit 13 Bit12 0 0 = Selected gate (external, external inverted, or software) rises 0 1 = Selected gate (external, external inverted, or software) falls 1 0 = External clock rises 1 1 = External clock falls	W
14	User Measure Enable Command The host should set up all the features/characteristics of the counter before issuing this command.	1 = Enables the selected measurement. 0 = Clears the measure enable flag.	W
15	Reserved[a]	–	–
16	Continuous Measure Mode The normal measure mode must also be selected to use this feature. A starting edge must be selected for this mode. The stop edge is not used.	1 = Enables continuous measure mode. 0 = Disables continuous measure mode	W

Table 13: User Control Registers (Addresses 0xB000C020, 0xB000C024, 0xB000C028) (cont.)

Bit	Register Description	Value	Type
17	Clear Continuous Measure Mode on Read Bit 16 must also be set to use this feature.	1 = Enables continuous measure mode to be cleared when read from the CGL address. 0 = Disables continuous measure mode from being cleared when read from the CGL address.	W
31:18	Reserved[a]	–	–

a. Bits for this register must always be written with 0. This allows these bits to be redefined as functional bits in the future without impacting existing software.

Table 14: User Status Register (Address 0xB000C030)

Bit	Register Description	Value	Type
0	User Counter 0 One-Shot Trigger Enable Flag This flag indicates whether user counter 0 is enabled to detect one-shot triggers. This bit resets to 0 on power up or counter/timer reset.	0 = One-Shot Triggers Disabled 1 = One-Shot Triggers Enabled This bit is set when the host writes 1 to the user one-shot trigger enable command bit of the control register. This bit is cleared by the core at the completion of the one-shot pulse if the counter is in non-retriggerable one-shot mode. It is also cleared when the user period register is loaded by the host.	R
1	User Counter 1 One-Shot Trigger Enable Flag This flag indicates whether user counter 1 is enabled to detect one-shot triggers. This bit resets to 0 on power up or counter/timer reset.	0 = One-Shot Triggers Disabled 1 = One-Shot Triggers Enabled This bit is set when the host writes 1 to the user one-shot trigger enable command bit of the control register. This bit is cleared by the core at the completion of the one-shot pulse if the counter is in non-retriggerable one-shot mode. It is also cleared when the user period register is loaded by the host.	R

Table 14: User Status Register (Address 0xB000C030) (cont.)

Bit	Register Description	Value	Type
2	User Counter 2 One-Shot Trigger Enable Flag This flag indicates whether user counter 2 is enabled to detect one-shot triggers. This bit resets to 0 on power up or counter/timer reset.	0 = One-Shot Triggers Disabled 1 = One-Shot Triggers Enabled This bit is set when the host writes 1 to the user one-shot trigger enable command bit of the control register. This bit is cleared by the core at the completion of the one-shot pulse if the counter is in non-retriggerable one-shot mode. It is also cleared when the user period register is loaded by the host.	R
3	Reserved	–	–
4	User Counter 0 Measure Enable Flag This signal indicates whether user counter/timer 0 is enabled to perform a measurement. This bit resets to 0 on power up or counter/timer reset.	0 = Measure Disabled 1 = Measure Enabled This bit is set when the host writes 1 to the user measure trigger enable command bit of the control register. This bit is cleared by the core at the completion of the measurement. It is also cleared when the host writes 0 to the user measure trigger enable command bit of the control register.	R

Table 14: User Status Register (Address 0xB000C030) (cont.)

Bit	Register Description	Value	Type
5	User Counter 1 Measure Enable Flag This signal indicates whether user counter/timer 1 is enabled to perform a measurement. This bit resets to 0 on power up or counter/timer reset.	0 = Measure Disabled 1 = Measure Enabled This bit is set when the host writes 1 to the user measure trigger enable command bit of the control register. This bit is cleared by the core at the completion of the measurement. It is also cleared when the host writes 0 to the user measure trigger enable command bit of the control register.	R
6	User Counter 2 Measure Enable Flag This signal indicates whether user counter/timer 2 is enabled to perform a measurement. This bit resets to 0 on power up or counter/timer reset.	0 = Measure Disabled 1 = Measure Enabled This bit is set when the host writes 1 to the user measure trigger enable command bit of the control register. This bit is cleared by the core at the completion of the measurement. It is also cleared when the host writes 0 to the user measure trigger enable command bit of the control register.	R
7	Reserved	–	–
31:8	Reserved	–	–

Counter/Timer Operation Modes

The following software-selectable modes are provided for each user counter/timer:

- **Retriggerable one-shot** – In retriggerable one-shot mode, an external gate rising or falling edge, or a transition from software logic low to software logic high can be used to trigger a pulse output signal.

  When the gate is active, the counter begins incrementing. When the counter increments to the value specified in the pulse register, the user output is activated. The user output stays active until the counter increments to the terminal count.

  The user output is then deactivated and the counter is automatically reloaded with the initial count, which is specified in the period register. The user output then stays inactive, and the counter stays disabled, until the next active gate signal. Note that all gates that occur while the counter is incrementing are ignored. The active polarity of the user output is software-selectable.

- **Non-retriggerable one-shot** – Non-retriggerable one-shot mode is the same as retriggerable one-shot mode with the following exception: when the counter reaches the terminal count, the module clears the one-shot trigger enable bit. The module ignores subsequent gate signals until the host sets the one-shot trigger enable bit.

- **Continuous increment (also known as divide by n)** – In continuous increment mode, an external gate high, external gate low, or software logic high can be used to enable the counter to increment.

  When the counter increments to the value specified in the pulse register, the user output is activated. The user output stays active until the counter increments to the terminal count. The user output is then deactivated and the counter is automatically

reloaded with the initial count, which is specified in the period register.

This sequence is repeated as long as the counter is enabled by the gate. The active polarity of the user output is software-selectable.

- **Measure** – Measure mode uses the internal clock to measure the time interval between the selected measure start edge and the selected measure stop edge. Either edge of the external gate or external clock can be independently chosen as the measure start edge or measure stop edge, providing the ability to measure the signal pulse width high, signal pulse width low, signal period, or time interval between two signals.

  Once the measure enable command is received from the host, the counter increments from the time it detects the selected measure start edge until it detects the selected measure stop edge. The counter then stops until it receives the next measure enable command from the host.

- **Continuous Measure** – Continuous measure mode uses the internal clock to measure the period of a signal on the external gate or external clock input. When the next edge is detected, the counter resets to 1 and starts counting again. Either a rising edge or falling edge can be used. The measurement count is latched and can be read from the CGL address of the counter. Setting bit 17 in the User Control registers, described in Table 13 starting on page 96, clears the measurement count after it is read and stays cleared until the next measurement is complete.

- **Up/Down** – In Up / Down mode, the counter increments (if the selected gate is active) or decrements (if the selected gate is inactive) on the rising edge of the clock. This mode should be used only with an external clock and external gate (normal or inverted).

  This mode is useful in monitoring the position of an object that can move in two directions, such as a lift on a shaker table. This mode does not support cascaded clocks.

The counter should be initialized such that the counter never increments beyond FFFFFFFFh or decrements below 0.

Up/down mode should be used only when the position of the object being monitored stays within the range of the counter, as the operation is not be reliable if the counter increments above FFFFFFFh or decrements below 0.

Count Sequence

The period register contains the initial count for the counter. When the host writes to the period register, the value written is immediately loaded into the counter. When the user counter counts, the counter increments from the initial count to the terminal count. When it reaches the terminal count, the counter is reloaded with the initial count. The terminal count is defined as 0. Therefore, the counter counts from period_reg to FFFFFFFFh, rolls over to 0, and then reloads to period_reg.

Event Counting Equations

When the user counter is used to count events, load the period register with a value from 1 to FFFFFFFFh. Use the following formula to determine the number of events that occurred:

events = ctr – period_reg

where *ctr* is the value read from the counter. For example, if reading the counter returns a value of 4, and *period_reg* = 1, three events occurred.

Output Period/Frequency Equations

When the user counter is used to generate an output signal, load the period register with a value from 1 to FFFFFFFFh. The following equations relate to the output period and frequency:

#clks per output period = FFFFFFFFh + 2 – period_reg

For example, if period_reg = FFFFFFFEh, three clocks occur for each output period. In this example, the counter counts FFFFFFFEh, FFFFFFFFh, 0, FFFFFFFEh, FFFFFFFFh, 0, and so on.

output period = (# clks per output period) x (clock period)

For example, if three clocks occur for each output period and the clock period is 55.555 ns, then the output period is 166.666 ns.

output frequency = 1 / output period

For example, if the output period is 166.666 ns, then the output frequency is 6.0 MHz.

Period_reg = FFFFFFFFh + 2 – (clock frequency / output frequency)

For example, if the clock frequency is 18 MHz and the desired output frequency is 6.0 MHz, the required period_reg is FFFFFFFEh.

Output Pulse Width and Duty Cycle Equations

The following equations relate to the output pulse width and duty cycle:

#clks per output pulse = FFFFFFFFh + 1 – pulse_reg

For example, if pulse_reg = FFFFFFFEh, two clocks occur for each output pulse. In this example, the output is active for counts FFFFFFFFh and 0.

Output pulse width = (#clks per output pulse) x (clock period)

For example, if the clock period is 55.55 ns and two clock occur for each output pulse, then the output pulse width is 111.11 ns.

Output duty cycle = (output pulse width) / (output period)

For example, if the output pulse width is 222.2 ns and the output pulse period is 333.3 ns, then the output duty cycle is 0.66 (66%).

Pulse_reg = FFFFFFFFh + 1 – (duty cycle x (clock frequency / output frequency))

For example, if the clock frequency is 18 MHz, the output frequency is 6.0 MHz, and the desired duty cycle is 2/3 (66%), then the required pulse_reg is FFFFFFFEh.

Counter Initialization

To initialize a counter / timer subsystem for continuous incrementing, do the following:

1. Select logic low for the gate source using the User Control registers, described in Table 13 on page 96.
2. Select the desired mode, output polarity and clock source using the User Control registers, described in Table 13 on page 96.
3. Load the User Period registers, described in Table 12 on page 94, with the desired value.
4. Load the User Pulse registers, described in Table 12 on page 94, with the desired value.
   Once loaded, the user counter/timer is waiting for an active gate to begin counting.
5. Select the desired gate using the User Control registers, described in Table 13 on page 96.
   If logic high is selected as the gate source, the counter/timer begins counting immediately. If an external gate is selected as the gate source, the counter counts when the external gate is active.

To initialize a counter / timer subsystem for an externally triggered one-shot operation, do the following:

1. Select logic low for the gate source using the User Control registers, described in Table 13 on page 96.
2. Select the desired mode, output polarity, and clock source using the User Control registers, described in Table 13 on page 96.
3. Load the User Period registers, described in Table 12 on page 94, with the desired value.
4. Load the User Pulse registers, described in Table 12 on page 94, with the desired value.
5. Select the desired gate in the User Control registers, described in Table 13 on page 96.

6. Issue a one-shot trigger enable command using the User Control registers, described in Table 13 on page 96.
   The user counter/timer waits for an active gate (trigger) to begin counting.

To initialize a counter/timer subsystem for a software triggered one-shot operation, do the following:

1. Select logic low for the gate source using the User Control registers, described in Table 13 on page 96.
2. Select the desired mode, output polarity, and clock source using the User Control register, described in Table 13 on page 96.
3. Load the User Period registers, described in Table 12 on page 94, with the desired value.
4. Load the User Pulse registers, described in Table 12 on page 94, with the desired value.
5. Issue a one-shot trigger enable command using the User Control registers, described in Table 13 on page 96.
   The user counter/timer waits for an active gate (logic high) to begin counting.
6. Select logic high for the gate source using the User Control registers, described in Table 13 on page 96.
   The counter begins counting.

Memory

All modules have 128 MBytes of SDRAM starting at address 0x80000000 through 0x81F40000 on the TMS230C6713. Additionally, 2 MB of flash memory starts at 0x90000000 (1 M x 16). This setup information is in the chip support library of Code Composer Studio.

Table 15 describes the memory space address map.

Table 15: Memory Space Address Map

Address	Register Description	Type
0x80000000	SDRAM, configured in the CDB file – CE0[a]	R/W
0x90000000	SDRAM1, configured in the CDB file – CE1[a]	R/W
0xB0000000	Hardware Control and Status Register – CE3	R/W
0xB0000004	Serial Control – Calibration – Termination Register	R/W
0xB0000008	Clock Divider Register (on DT9842/2 and DT9842/8 modules only)	R/W
0xB0001000	Board ID (upper 16 bits) and FPGA revision (lower 16 bits)	R
0xB0004000	A/D Data Channel 0 (Left Justified Data)	R
0xB0004004	A/D Data Channel 1 (Left Justified Data)	R
0xB0004008	A/D Data Channel 2 (Left Justified Data)	R
0xB000400C	A/D Data Channel 3 (Left Justified Data)	R
0xB0004010	A/D Data Channel 4 (Left Justified Data)	R
0xB0004014	A/D Data Channel 5 (Left Justified Data)	R
0xB0004018	A/D Data Channel 6 (Left Justified Data)	R
0xB000401C	A/D Data Channel 7 (Left Justified Data)	R

Table 15: Memory Space Address Map (cont.)

Address	Register Description	Type
0xB0004020	Flags, Digital Port 2[b], Digital Port 1, Digital Port 0	R
0xB0004024	Counter Timer 0	R
0xB0004028	Counter Timer 1	R
0xB000402C	Counter Timer 2	R
0xB0004030[c]	Firmware Debug	R/W
0xB0008000	D/A Data 0 (Left Justified Data)	W
0xB0008004	D/A Data 1 (Left Justified Data)	W
0xB0008008	Reserved "0s," Digital Port 2[b], Digital Port 1, Digital Port 0	W
0xB000C000	User Period Register 0/ Counter 0	R/W
0xB000C004	User Period Register 1/ Counter 1	R/W
0xB000C008	User Period Register 2/ Counter 1	R/W
0xB000C00C	Reserved	–
0xB000C010	User Pulse Register 0	W
0xB000C014	User Pulse Register 1	W
0xB000C018	User Pulse Register 2	W
0xB000C01C	Reserved	–
0xB000C020	User Control 0	W
0xB000C024	User Control 1	W
0xB000C028	User Control 2	W
0xB000C02C	Reserved	–
0xB000C030	Counter Timer Status	R

Table 15: Memory Space Address Map (cont.)

Address	Register Description	Type
0xB0010000	Digital Port 0 INT Mask Register (Right Justified Data)	R/W
0xB0010004	Digital Data Port 0 (Right Justified Data)	R/W
0xB0010008	Digital Data Port 1 (Right Justified Data)	R/W
0xB001000C	Digital Data Port 2 (Right Justified Data)	R/W
0xB0014000	SB Control & Address Register – CE3	R/W
0xA0000000	16-Bit SB Data Register – CE2 (20 ns; set up for 2 cycles)	W
0xA0000004	16-Bit SB Data Register – CE2 (20 ns; ECLKIN/2)	R

a. Refer to the *DT9840 Series DSP Library User's Manual* for more information on the CDB file.

b. For the DT9841-VIB module, bit 0 of digital port 2 is used as the SCL clock, and bit 1 of digital port 2 is used as the SDA data output; the remaining bits (2-7) of digital port 2 are reserved. See page 75 for more information.

c. This register contains eight debug LEDs that are right-hand justified. Debug LEDs are not supported on the DT9841E. Bits 0 (D0) through 7 (D7) correspond to LEDs CR5 through CR12. (The LEDs were numbered differently on some early modules.)

   If an error is detected in a running DT9840 Series DSP program, these LEDs turn on.

Scalable Bus

Note: The Scalable Bus is not supported by DT9841E modules.

Two 50-pin connectors (J12 and J13) on the DT9840 Series module provide the a Scalable Bus for connecting modules together. By plugging EP342 cables from one module to another, you can connect up to seven "slave" modules to a DT9840 Series "master" module. The first module (usually the master) and the final module (usually a slave) in the chain must be terminated in software with 100 ohms. Bit 25 of the Calibration and Setup register, described in Table 6 on page 75, controls the 100 ohm termination resistors.

The Scalable Bus connector is set up for intermodule communication at speeds up to 50 MBytes/s (note however, that the maximum rate in software is 11.3 MBytes/s). The negative strobe pulse must be 12 ns minimum with the data valid for 10 ns before the rising edge. The hold time is 0 ns.

When a slave module requests service, it asserts interrupt EXT_INT4. The master module reads each slave at a time to determine which module asserted the interrupt line. The requesting module places the number of words to transfer on the bus. All other modules place zeros on the bus. The module is now set up to write the number of words reported.

The SB Control register, described in Table 16, is used to control the operation of the Scalable Bus.

Table 16: SB Control Register (Address 0xB0014000)

Bit	Register Description	Type
0 to 2[a]	These are the slave addresses for modules 1 through 7. For slaves, set these bits to a unique address for the module. For the master, set these bits to 000.	R/W
3	1 = The module is the master (determined at initial setup). The master determines if each slave module is reading from or writing to the Scalable Bus. 0 = The module is a slave.	R/W
4	1 = Broadcast mode. In broadcast mode, the master writes to all slaves. 0 = Broadcast mode is not used.	R/W
5	1 = The master writes to the selected address with a 40.0 ns delay between writes. (Refer to CE2 described on page 112. The 40 ns delay is implemented using two cycles in the write setup. 0 = A read operation is performed. (Slaves are read-only devices).	R/W
6	Reserved	–
7[b]	1 = Enable transfer request (Ack Out)/acknowledge strobe. After the modules are set up, the enable is asserted 200 ns later to deglitch the setup operation. The Scalable Bus is now activated and data can be transferred at full bus rates. When the master finishes reading a single word of Transfer Request, it generates a pulse on this line (write bit to 1, then 0). (Slaves are read-only devices). 0 = Disable transfer request/acknowledge strobe.	R/W

Table 16: SB Control Register (Address 0xB0014000) (cont.)

Bit	Register Description	Type
8	1 = The FIFO is half full on the slave or the master when the slave is writing to the Scalable Bus. Interrupt EXT_INT7 is asserted for 512 DMA transfers to memory. 0 = The FIFO is not half full on the Scalable Bus.	R
9	1 = The FIFO is not empty on the Scalable Bus. After the transfer is completed, this bit must be checked to ensure that all the data has been read. 0 = The FIFO is empty on the Scalable Bus.	R
10	1 = A FIFO error occurred on the Scalable Bus. 0 = A FIFO error did not occur on the Scalable Bus.	R
11	1 = Transfer request strobe output. The slave interrupts the master to indicate a transfer request. Also used to handshake the three word transfer request to the master. (Read-only for master.) 0 = No transfer request from slave.	R/W
12	1 = Transfer request strobe latch. Latches the signal on bit 11. 0 = Clears the transfer request strobe latch.	R/W
13	1 = Latch transfer request (Ack In). Latches the signal on bit 7. 0 = Clears the latch transfer request.	R/W
14	1 = Enable transfer request interrupt. Enable the transfer request strobe to generate an interrupt on EXT_INT4 on the master. 0 = Disable transfer request interrupt.	R/W

Table 16: SB Control Register (Address 0xB0014000) (cont.)

Bit	Register Description	Type
15	1 = The address on the Scalable Bus matches the address of the slave. 0 = The address on the Scalable Bus does not match the address of the slave.	R
16 - 18	Bus Address Bits (Master Only) Set these bits to the address of the slave with which the master will communicate.	R/W
19	1 = Enable the Receive FIFO bit on the master. 0 = Disable the Receive FIFO bit on the master.	R/W
20	1 = Enable writing to the FIFO on the slave module as long as the slave is addressed or a broadcast message is sent on the bus. 0 = Disable writing to the FIFO on the slave module.	R/W
21 - 31	Reserved	–

a. Bits 0 through 3 are written by the host / USB to specify the module as a master or slave and to set the address of the slaves. Four address LEDs (CR15) indicate the Scalable Bus address; position M is the master and positions 1, 2, and 4 are turned on as needed to represent the slave address. The intensity of the LEDs for the addressed module is brighter than the LEDs for the nonaddressed modules. The Scalable Bus is not supported by the DT9841E.

b. When a master finishes reading a single word of Transfer Request, the master generates a pulse on this line (write bit set to 1 then to 0).

Table 17 describes the SB Write Data Address and Read Data Address registers.

Table 17: SB Write Data Address and Read Data Address Registers

Address	Register Name	Register Description	Type
0xA0000000	Write Data Address	Bits 0 to 15 contain the data locations for the Scalable Bus. The master module writes to address 0xA000A000 on the selected slave with a 40.0 ns delay between writes (ECLKIN divided by 2 + 2 setup). After 512 16-bit words are written, the FIFO half full flag on the addressed slave asserts interrupt EXT_INT7 for a 512 sample transfer to memory using DMA channel 7. When the module address is removed (indicating that the transfer is done), the slave module checks the FIFO not empty flag to complete the data transfer.	W
0xA0000004	Read Data Address	Once the Enable bit is set, the selected slave can write to the master through the Scalable Bus in the same manor as the master writes to the slave. The only exception is that the first data point is the number of samples in the data file to be transferred. If the slave module needs to send data to the master, it asserts DONE_L, which asserts interrupt EXT_INT4. The master then queries each slave for the request. When the slave module is addressed, the first data point is the number of samples in the data file to be transferred. The data is then written from the slave to the master. If the selected slave did not request the bus, then all zeros are placed in the bus.	R

3

Calibration

Use the DT9841 Calibration Utility to calibrate the analog input and analog output circuitry on the DT9841, DT9841E, and DT9841-VIB modules.

Note: The DT9841 Calibration Utility is not supported by DT9842/2 and DT9842/8 modules.

This chapter describes how to calibrate the analog input and output subsystems of a DT9841, DT9841E, or DT9841-VIB module using the DT9841 Calibration Utility.

Using the DT9841 Calibration Utility

Note: Ensure that you installed the DT9840 Series software prior to using the DT9841 Calibration Utility. Refer to the *DT9840 Series Getting Started Manual* for more information on installing the software.

Start the DT9841 Calibration Utility as follows:

1. Double-click **DT9841 Calibration Utility** (located under Start \ Programs \ Data Translation, Inc. \ DT9840 Series).
   The main menu appears.
2. Select the DT9841, DT9841E, or DT9841-VIB module to calibrate, and then click **OK**.
   The firmware is downloaded to the module and the calibration utility starts after a few seconds.

Once the DT9841 Calibration Utility is running, you can calibrate the analog input circuitry (either automatically or manually), described on page 122, or the analog output circuitry of the DT9841, DT9841E, or DT9841-VIB module, described on page 126.

Calibrating the Analog Input Subsystem

This section describes how to use the DT9841 Calibration Utility to calibrate the analog input subsystem of a DT9841, DT9841E, or DT9841-VIB module.

Connecting a Precision Voltage Source

To calibrate the analog input circuitry, you need to connect an external +9.3750 V precision voltage source to the analog input channels of a DT9841, DT9841E, or DT9841-VIB module.

Using the Auto-Calibration Procedure

Auto-calibration is the easiest to use and is the recommended calibration method. To auto-calibrate the analog input subsystem, do the following:

1. Select the **A/D Configuration** tab of the DT9841 Calibration Utility.
2. In the Clock Frequency edit box, enter a clock frequency between 5 kHz and 100 kHz at which you will be operating the module.

Note: The calibration changes at different clock frequencies, so it is important that you specify the clock frequency at which you will be operating the module.

If you later change the operating clock frequency, recalibrate the A/D channels.

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3. In the A / D Channel Select section, select the A / D channels that you want to calibrate by clicking the checkboxes next to the channel numbers. Each DT9841 channel must be calibrated separately.

4. Click **Start Auto Calibration**.
   You are prompted to verify that 0V is applied to the first selected channel.

5. Connect a precision voltage source to the first selected analog input channel, verify that 0 V is applied to the channel, and then click **OK**.
   The offset value is calibrated. When the offset calibration is complete, a message appears notifying you to set the input voltage of the first A/D channel to +9.375 V.

6. Apply a voltage of +9.375V to the selected A / D channel, and then click **OK**.
   The gain value is calibrated.

7. Connect a precision voltage source to the next selected analog input channel, verify that 0 V is applied to the channel, and then click **OK**.
   The offset value is calibrated. When the offset calibration is complete, a message appears notifying you to set the input voltage of the first A/D channel to +9.375 V.

8. Apply a voltage of +9.375V to the selected A / D channel, and then click **OK**.
   The gain value is calibrated.

9. Repeat steps 7 and 8 until all the selected analog input channels are calibrated.
   When the last channel has been calibrated, a completion dialog box is displayed.

10. Click **OK** to finalize the analog input calibration process.

Note: At any time, you can click **Restore Factory Settings** to reset the A / D calibration values of the selected channels only to their original factory settings. This process will undo any auto or manual calibration settings.

Using the Manual Calibration Procedure

If you want to manually calibrate the analog input circuitry instead of auto-calibrating it, do the following:

1. In the Clock Frequency edit box, enter a clock frequency between 5 kHz and 100 kHz at which you will be operating the module.

   Note: The calibration changes at different clock frequencies, so it is important that you specify the clock frequency at which you will be operating the module.

   If you later change the operating clock frequency, recalibrate the A / D channels.

2. In the Manual Calibration section, select an A / D channel to calibrate.
3. Adjust the offset as follows:
   - **r.** Verify that 0 V is applied to the selected channel.
     The current voltage reading for this channel is displayed in the A/D Value window.
   - **s.** Adjust the offset by entering values between 0 and 255 in the Offset edit box, or by clicking the up / down buttons until the A / D Value is 0.000 V.

4. Adjust the gain as follows:

   a. Verify that +9.375V is applied to the selected A / D channel. *The current voltage reading for this channel is displayed in the A/D Value window.*

   b. Adjust the gain by entering values between 0 and 255 in the Gain edit box, or by clicking the up / down buttons until the A / D Value is 9.3750.

5. Repeat steps 2 through 4 for each A / D channel that you wish to calibrate manually.

Note: At any time, you can click **Restore Factory Settings** to reset the A / D calibration values of the selected channels only to their original factory settings. This process will undo any auto or manual calibration settings.

Once you have finished this procedure, continue with "Calibrating the Analog Output Subsystem" on page 126.

Calibrating the Analog Output Subsystem

This section describes how to use the DT9841 Calibration Utility to calibrate the analog output subsystem of a DT9841, DT9841E, or DT9841-VIB module.

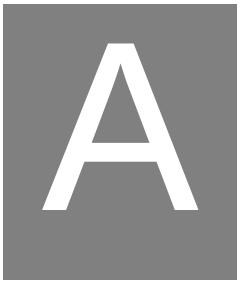
To calibrate the analog output circuitry, you need to connect an external precision voltmeter to the analog output channels of the DT9841, DT9841E, or DT9841-VIB module.

Do the following to calibrate the analog output circuitry:

1. Select the D / A Configuration tab of the DT9841 Calibration Utility.
2. Connect an external precision voltmeter to Analog Output 0 (DAC Ch0) of the DT9841, DT9841E, or DT9841-VIB module.
3. In the DAC Output Voltage box, select **0 V**.
4. Adjust the offset by entering values between 0 and 255 in the DAC 0 Offset edit box or by clicking the up / down buttons until the voltmeter reads 0 V.
5. In the DAC Output Voltage box, select **9.375 V.**
6. Adjust the gain by entering values between 0 and 255 in the DAC 0 Gain edit box or by clicking the up / down buttons until the voltmeter reads 9.375 V.
7. Connect an external precision voltmeter to Analog Output 1 (DAC Ch1) of the DT9840 Series module.
8. In the DAC Output Voltage box, select **0 V**.
9. Adjust the offset by entering values between 0 and 255 in the DAC 1 Offset edit box or by clicking the up / down buttons until the voltmeter reads 0 V.
10. In the DAC Output Voltage box, select **9.375 V**.
11. Adjust the gain by entering values between 0 and 255 in the DAC 1 Gain edit box or by clicking the up / down buttons until the voltmeter reads 9.375 V.

Note: At any time, you can click **Restore Factory Settings** to reset the D/A calibration values of both DACs to their original factory settings. This process will undo any D/A calibration settings.

Once you have finished this procedure, the analog output circuitry is calibrated. To close the DT9841 Calibration Utility, click the close box in the upper, right corner of the window.



Specifications

Table 3 lists the specifications for the analog input subsystem.

Table 3: Analog Input Subsystem Specifications

Feature	DT9841, DT9841E, and DT9841-VIB Specifications	DT9842/2 and DT9842/8 Specifications
Number of analog inputs	**For DT9841:** 8 differential, simultaneously sampled and held (SSH) **For DT9841E:** 2 differential, simultaneously sampled and held (SSH) **For DT9841-VIB:** 8 single-ended, simultaneously sampled and held (SSH)	8 single-ended, simultaneously sampled and held (SSH)
Number of gains	1 (the value is always 1)	1 (the value is always 1)
Resolution	24 bits	16 bits
Data encoding	Twos complement	Twos complement
System accuracy (full-scale)	**For DT9841 and DT9841E:** 0.024% **For DT9841-VIB:** 0.044%	0.02%
Nonlinearity (integral)	±4096 LSBs	±0.01%
Differential linearity (monotonic)	±64 LSBs	±1 LSB

A

Table 3: Analog Input Subsystem Specifications (cont.)

Feature	DT9841, DT9841E, and DT9841-VIB Specifications	DT9842/2 and DT9842/8 Specifications
1 LSB	1.192 µV (20 V/2^{24})	305 µV (20 V/2^{16})
Input signal range	±10 V	±10 V
Coupling	**For DT9841 and DT9841E:** DC **For DT9841-VIB:** AC –3dB: 1.6 Hz DC offset: 1.5 mV	DC
Zero error	±0.001 V	±0.001
Drift Zero: Gain:	 ±40 µV/° C ±100 ppm/° C	 ±20 µV/° C ±25 ppm/° C
Input impedance	**For DT9841 and DT9841E:** 100 MΩ, 10 pF **For DT9841-VIB:** 1 MΩ, 20 pF[a]	100 MΩ, 10 pF
Input bias current	±10 nA	±10 nA
Common mode voltage	±11 V maximum (operational)	±11 V maximum (operational)

Table 3: Analog Input Subsystem Specifications (cont.)

Feature	DT9841, DT9841E, and DT9841-VIB Specifications	DT9842/2 and DT9842/8 Specifications
Maximum input voltage	**For DT9841 and DT9841E:** ±25 V maximum (protection DC) **For DT9841-VIB:** ±40 V maximum (protection DC)	±25 V maximum (protection DC)
Internal reference	+2.5 V ±0.002 V	+2.5 V ±0.002 V
A/D converter noise	16 LSBs rms	0.75 LSBs rms
Channel-to-channel offset	±700 µV	±700 µV
Channel-to-channel aperture match	±5 ns	±3 ns
Aperture jitter	100 ps rms	10 ps rms
A/D conversion time	10 µs	8 µs
A/D type	Delta-Sigma	Successive Approximation
Group delay (DT9841, DT9841E, and DT9841-VIB)	370 µs @ 100 kHz (37/Throughput)	–
Pass-band	0.453 x Throughput	–
Stop-band	0.547 x Throughput	–
Signal/(Noise + Distortion)	-92 db @ 1 kHz	-86 db @ 1 kHz
Total Harmonic Distortion	-96 db @ 1 kHz	-90 db @ 1 kHz
Spurious Free Dynamic Range	110 dB	90 dB

Table 3: Analog Input Subsystem Specifications (cont.)

Feature	DT9841, DT9841E, and DT9841-VIB Specifications	DT9842/2 and DT9842/8 Specifications
Channel crosstalk	–100 dB @ 1 kHz	–100 dB @ 1 kHz
Data Throughput Single channel: Scan all channels:	 100 kS/s **For DT9841 and DT9841-VIB:** 800 kS/s **For DT9841E:** 200 kS/s	 100 kS/s 800 kS/s
Accuracy of Clock Oscillator	0.01%	0.01%
IEPE Current Source (DT9841-VIB)	4 mA	–
IEPE Current Source Noise (DT9841-VIB)	10 nA rms @ 1 kHz	–
IEPE Compliance Voltage (DT9841-VIB)	24 V	–
IEPE Current Source Accuracy (DT9841-VIB)	±1.0%	–
IEPE Filter (DT9841-VIB)	2-pole, Butterworth 10 kHz (–3 dB)	–

a. Cable capacitance of typically 30 pF per foot must be added.

Table 4 lists the specifications for the analog output subsystem.

Table 4: Analog Output Subsystem Specifications

Feature	DT9841, DT9841E, and DT9841-VIB Specifications	DT9842 Specifications
Number of analog output channels	2	2 for DT9842/2 8 for DT9842/8
Resolution	24 bits	16 bits
Data encoding	Twos complement	Offset binary
Nonlinearity (integral)	±1024 LSBs	±0.01%
Differential linearity	±64 LSBs	±1 LSB
Zero error	Software-adjustable to zero	Software-adjustable to zero
Gain error	±2048 LSBs	±2 LSBs
Output ranges	±10 V and ±2.5 V (bipolar)	±10 V (bipolar)
Throughput (full-scale)	100 kHz	100 kHz
Current output	±5 mA minimum (10 V/ 2 kΩ)	±5 mA minimum (10 V/ 2 kΩ)
Output impedance	0.3 Ω typical	0.3 Ω typical
Capacitive drive capability	0.001 µF minimum (no oscillations)	0.001 µF minimum (no oscillations)
Protection	Short circuit to analog common	Short circuit to analog common
Power-on voltage	0 V ±10 mV maximum	0 V ±10 mV maximum

A

Table 4: Analog Output Subsystem Specifications (cont.)

Feature	DT9841, DT9841E, and DT9841-VIB Specifications	DT9842 Specifications
Settling time to 0.01% of FSR (filtering off)	10 µs, 20 V step	10 µs, 20 V step
Total harmonic distortion	-94 dB	-88 dB
Glitch area	–	10 nV - Seconds, typical
Slew rate	5 V/µs	5 V/µs
Group delay 34/conversion rate	340 µs @ 100 kHz	–
Passband	0.454 x Throughput	–
Stopband	0.546 x Throughput	–
Pass-band ripple	±0.002 dB	–
Software-selectable 4-pole filter	20 kHz or 5 kHz	–
FIFO	DSP memory	DSP memory

Table 5 lists the specifications for the digital input subsystem.

Table 5: Digital Input Subsystem Specifications

Feature	Specifications
Number of lines	**For DT9841-VIB:** 16 (Ports 0 and 1, each consisting of 8 programmable digital I/O lines)[a] **For all other DT9840 Series modules:** 24 (Ports 0, 1, and 2, each consisting of 8 programmable digital I/O lines)[a]
Termination	22 kΩ pull-up series 22 Ω
Input type	HCT
+5 V tolerant	Yes
Input load	22 kΩ pull-up to 3.3 V
Inputs Input type: Input load: High-level input voltage: Low-level input voltage: High-level input current: Low-level input current:	 Level sensitive 1 (HCT) 2.4 V minimum 0.8 V maximum 0 µA 0.2 mA
Back EMF diodes	Yes

a. When port 0 is configured for digital input, you can configure the software to interrupt the host computer whenever any of the bits changes state. In addition, to reduce noise and minimize false state changes, you can enable a 10 ms deglitch function for port 0 when it is configured for digital input.

Table 6 lists the specifications for the digital output subsystem.

Table 6: Digital Output Subsystem Specifications

Feature	Specifications
Number of lines	**For DT9841-VIB:** 16 (Ports 0 and 1, each consisting of 8 programmable digital I/O lines) **For all other DT9840 Series modules:** 24 (Ports 0, 1, and 2, each consisting of 8 programmable digital I/O lines)
Termination	22 kΩ pull-up series 22 Ω
Outputs Output driver: Output driver high voltage: Output driver low voltage:	 CMOS 22 kΩ pull-up to 3.3 V 0.4 V @ 10 mA
Back EMF diodes	Yes

Table 7 lists the specifications for the C/T subsystems.

Table 7: C/T Subsystem Specifications

Feature	Specifications
Number of counter/timer channels	3
Clock Inputs Input type: High-level input voltage: Low-level input voltage: +5 V tolerant Minimum pulse width: Maximum frequency:	 HCT with 22 kΩ pull-up to 3.3 V 2.4 V minimum 0.8 V maximum Yes 25 ns (high); 25 ns (low) 20 MHz
Gate Inputs Input type: High-level input voltage: Low-level input voltage: +5 V tolerant Minimum pulse width:	 HCT with 22 kΩ pull-up to 3.3 V 2.4 V minimum 0.8 V maximum Yes 25 ns (high); 25 ns (low)
Counter Outputs Output driver high voltage: Output driver low voltage:	 3.0 V minimum @ 0.1 mA Source 0.4 V maximum @ 2 mA Sink

Table 8 lists the specifications for the external clock signal to the DT9840 Series modules.

Table 8: External Clock Specifications

Feature	Specifications
Input type	HCT Rising-Edge Sensitive with 22 kΩ pull-up resistor
High-level input voltage	2.4 V minimum
Low-level input voltage	0.8 V maximum
Minimum pulse width	9 ns (high); 9 ns (low)
Maximum frequency DT9841 and DT9841E: DT9842/2 and DT9842/8:	 51.2 MHz[a] 100 kHz

a. For the DT9841 and DT9841E, the conversion rate = Clock frequency / 512

Table 9 lists the specifications for the external trigger signal to the DT9840 Series modules.

Table 9: External Trigger Specifications

Feature	Specifications
Input type	HCT Rising-Edge Sensitive with 22 kΩ pull-up resistor
High-level input voltage	2.4 V minimum
Low-level input voltage	0.8 V maximum
Minimum pulse width	50 ns (high); 50 ns (low)
Maximum frequency	50.0 kHz

Table 10 lists the power, physical, and environmental specifications for the DT9840 Series modules.

Table 10: Power, Physical, and Environmental Specifications

Feature	Specifications
Power	
+5 V ±0.25 V:	**DT9841-VIB:** 4 A maximum (3.3 A typical); (300 mA maximum for IEPE functions) **All other DT9840 Series modules:** 5 A maximum (3 A typical)
+5 V Isolated Power Out:	**DT9841-VIB:** 700 mA **All other DT9840 Series modules:** 1 A maximum
Physical	
Dimensions	
Board-Level Version:	**DT9841E:** 280 x 100 x 22 mm **All other DT9840 Series modules:** 233.35 mm x 220 mm
Sleek Box:	229 mm (L) x 247 mm (W) x 114 mm (H)
Weight:	
Board-Level Version:	**DT9841E:** 0.492 lb. (223 g.) **All other DT9840 Series modules:** 1.572 lbs (713 g)
Sleek Box:	5.85 lbs (2.654 kg)

Table 10: Power, Physical, and Environmental Specifications (cont.)

Feature	Specifications
Environmental	
Operating temperature range:	0° C to 55° C
Storage temperature range:	-25° C to 85° C
Relative humidity:	To 95%, noncondensing
Altitude:	10,000 feet

Table 11 lists the regulatory specifications for the DT9840 Series modules.

Table 11: Regulatory Specifications

Feature	Specifications
EMI	FCC part 15, class A EN 55022:1994 (based on CISPR-22:1993)
EN 50082-1:1998	
IEC 801-2:1984:	8 KV air/4 KV contact
IEC 801-3:	3 V/m from 27 to 500 MHz
IEC 801-4:	1 KV coupled to AC lines 0.5 KV coupled to I/O lines
VCCI (Japan version of CISPR-22)	
Safety:	UL, CSA
RoHS (EU Directive 2002/95/EG)	Compliant (as of July 1st, 2006)

Table 12 lists the specifications for the connectors on the DT9840 Series modules, Sleek Box, EP358E, and EP342 and EP344 cables.

Table 12: DT9840 Series Connector Specifications

Product	Connector	Connector Part Number	Mating Connector Part Number
Sleek Box	Analog Input (J1)	AMP/Tyco 5747375-8	AMP/Tyco 5-747917-2
	Digital I/O (J2)	AMP/Tyco 5747301-8	AMP/Tyco 5-747916-2
	Counter/Timer (J19)	AMP/Tyco 5745967-8	AMP/Tyco 5-747912-2
	J201 and J202 (behind front panel)	AMP/Tyco 6-104068-8	AMP/Tyco 3-111196-4
	Scalable Bus (J12 and J13)	3M N10250-52E2PC	3M 10150-6000EC
	Serial Port (J4)	AMP/Tyco 5747844-4	AMP/Tyco 5-747904-2
	+5 V Power Input (J11[b])	Kycon KPJX-4S-S	Kycon KPPX-4P
	USB (J6)	AMP/Tyco 292304-2	Data Translation EP365 USB cable or AMP/Tyco 1487588-3
DT9841, DT9842/2, DT9842/8 (Board-Level Version)	TB3[a], Ext. Fan TB4, +5 V Power Output	PCD ELVH02500	PCD ELVP02100
	J3	AMP/Tyco 5-146130-6	Blackhawk JTAG emulator
	J4	AMP/Tyco 5747844-4	AMP/Tyco 5-747904-2
	J6	AMP/Tyco 292304-2	Data Translation EP365 USB cable or AMP/Tyco 1487588-3
	TB1, +5 V Power Output	Tyco/Buchanan 796644-2	Tyco/Buchanan 796640-2

Table 12: DT9840 Series Connector Specifications (cont.)

Product	Connector	Connector Part Number	Mating Connector Part Number
DT9841, DT9842/2, DT9842/8 (Board-Level Version, cont.)	J11[b]	Kycon KPJX-4S-S	Kycon KPPX-4P
	J12 and J13	3M N10250-52E2PC	3M 10150-6000EC
	J15 and J16 - BNCs	Molex 73101-0161	AMP/Tyco 1-221265-1
	J17 and J18	AMP/Tyco 6-104068-8	AMP/Tyco 3-111196-4
DT9841E (Board-Level Version)	J1 and J2	AMP/Tyco 6-104068-8	AMP/Tyco 3-111196-4
	J3	AMP/Tyco 5-146130-6	Blackhawk JTAG emulator
	J4	3M 30310-6002HB	3M 89110-0101
	J6	AMP 292304-2	Data Translation EP365 USB cable or AMP/Tyco 1487588-1
	J11[b]	Kycon KPJX-4S-S	Kycon KPPX-4P
	TB2	Phoenix Contact 1707434	Phoenix Contact 1839610
	TB3	PCD ELVH02500	PCD ELVP02100
EP358E	Analog Input (J1)	AMP/Tyco 5747375-8	AMP/Tyco 5-747917-2
	Digital I/O (J2)	AMP/Tyco 5747301-8	AMP/Tyco 5-747916-2
	Counter/Timer (J19)	AMP/Tyco 5745967-8	AMP/Tyco 5-747912-2
	J201 and J202 (behind front panel)	AMP/Tyco 6-104068-8	AMP/Tyco 3-111196-4

Table 12: DT9840 Series Connector Specifications (cont.)

Product	Connector	Connector Part Number	Mating Connector Part Number
EP344	Both connectors	AMP/Tyco 3-111196-4	AMP/Tyco 6-104068-8
EP354	Connector that attaches to the DT9840 Series module or Sleek Box	AMP/Tyco 5-747904-2	AMP/Tyco 5747844-4
	Connector that attaches to the EP335 cable[c]	AMP/Tyco 747905-7	Male, 9-pin, D-sub connector of the EP335 cable[c]

a. The following fan is recommended for use withTB3: Sunon model number KDE0505PFB3-8GN.
b. The following power supply is recommended: Total Power International model number TPES49-05060KPP-4P or Data Translation part number 19481 (EP348).
c. This cable, which is included with the EP354 serial adapter, is also available as an off-the-shelf product from Assmann (part number AK131-2-R). This cable has a male, 9-pin, D-sub connector on one end and a female, 9-pin, D-sub connector on the other end.

B

Connector Pin Assignments

DT9841, DT9842/2, and DT9842/8 Modules

The DT9841, DT9842/2, and DT9842/8 modules provide the following connectors:

- Connector J2 – a 2-pin connector provided for attaching an external +5 VDC, 100 mA fan output signal. The fan will turn on with an onboard temperature sensor if the DT9840 Series module exceeds 45° C. If the module exceeds 60° C, an interrupt is generated. The following fan is recommended: Sunon model number KDE0505PFB3-8GN or Data Translation part number 19372. Refer to Table 13 on page 148 for more information on this connector.
- Connector J3 – a 14-pin connector provided for a JTAG device, such as a Blackhawk emulator. Refer to Table 14 on page 149 for more information on this connector.
- Connector J4 – a 9-pin, D-shell connector provided for attaching an RS-232-compliant device for debugging purposes using the EP354 serial adapter and EP335 cable. Refer to the *DT9840 Series Getting Started Manual* for connection information and to the *DT9840 Series DSP Library User's Manual* for information about the serial debugging functions.

Note: Refer to Table 15 on page 149 for more information on the pin assignments for this connector.

This serial port (serial port 1 (McBSP) of the DSP) can also be programmed for several modes of operation at bit rates of up to 33 Mbps. Refer to the data sheet for the TMS320C6713 from Texas Instruments (part number SPRS088F) for more information on programming the serial port.

- Connector J6 – a 4-pin USB connector. Refer to Table 16 on page 150 for more information on this connector.

- Connector J11 – a 4-pin locking connector provided for attaching an external +5 V power input signal. Refer to Table 17 on page 151 for more information on this connector.

Note: You must consider the wire size and length before connecting power to connector J11. The module requirement is +5 V ±0.25 V at the connector with less than 50 mV pp of ripple. The power supply must also be isolated from the computer or from the power commons up to 500 V minimum. The following power supply is recommended: Total Power International number TPES49-05060KPP-4P or Data Translation EP348 (part number 19481).

- Connectors J12 and J13 – 50-pin, Scalable Bus connectors for attaching additional DT9840 Series modules.

  Each Scalable Bus connector is set up for intermodule communication at speeds up to 50 MBytes/s (maximum software rate is 13 MBytes/s). The first and last modules must use software-selectable 100 Ω termination resistors. The data can be clocked out every 40 ns. The negative strobe pulse must be 12 ns minimum with the data valid for 10 ns before the rising edge. The hold time is 0 ns.

  Refer to Table 18 on page 151 for more information on these connectors.

- Connectors J15 and J16 – The BNC connector labelled J15 is provided for attaching an external clock to the module; the BNC connector labelled J16 is provided for attaching an external trigger.

- Connector J17 – a 68-pin connector provided for attaching analog output, digital I/O, and counter/timer signals. Refer to Table 19 on page 153 for more information on this connector.

- Connector J18 – a 68-pin connector provided for attaching analog input signals. Refer to Table 20 on page 155 for more information on this connector.
- Connector J19 – a 2-pin connector provided for attaching and external +5 V output signal. Refer to Table 21 on page 156 for more information on this connector.

Note: You can use the 2-position terminal block TB1 instead of connector J19, if you wish.

- Screw terminal block – TB1 is provided for attaching an external +5 V power output signal. Refer to Table 22 on page 157 for more information on the screw terminal block assignments.

Note: You can use connector J19 instead of screw terminal block TB1, if you wish.

Table 13: Fan Output Connector (J2) Pin Assignments

Pin	Signal Name[a]
1	Fan+
2	Fan–

a. These signals are provided for attaching an external +5 VDC, 100 mA fan output signal. The fan will turn on with an onboard temperature sensor if the DT9840 Series module exceeds 45° C. If the module exceeds 60° C, an interrupt is generated. The following fan is recommended: Sunon model number KDE0505PFB3-8GN or Data Translation part number 19372.

Table 14: JTAG Connector (J3) Pin Assignments

Pin	Signal Name	Pin	Signal Name
1	DSP_TMS	2	DSP_TRST_N
3	DSP_TDI	4	DGND
5	+3.3 V	6	Not Connected
7	DSP_TDO	8	DGND
9	DSP_TCK	10	DGND
11	DSP_TCK	12	DGND
13	DSP_EMU0	14	DSP_EMU1

Table 15: Serial Port Connector (J4) Pin Assignments

J4. Pin	Signal Name[a]	Signal Description	McBSP Pin	McBSP Function	McBSP Internal Pull Up or Pull Down
1	CLKS1	External Clock Source	E1	Input	Internal Pull Down
2	DR1	Receive Data	M2	Input	Internal Pull Up
3	DX1	Transmit Data	L2	Output/ Tristate	Internal Pull Up
4	CLKR1	Receive Clock	M1	Input/Output/ Tristate	Internal Pull Down
5	Isolated Common	Ground	–	–	–
6	CLKX1	Transmit Clock	L3	Input/Output/ Tristate	Internal Pull Down

Table 15: Serial Port Connector (J4) Pin Assignments (cont.)

J4. Pin	Signal Name[a]	Signal Description	McBSP Pin	McBSP Function	McBSP Internal Pull Up or Pull Down
7	FSX1	Transmit Frame Sync	L1	Input/Output/ Tristate	Internal Pull Down
8	FSR1	Receive Frame Sync	M3	Input/Output/ Tristate	Internal Pull Down
9	+5 V_PWR	+5 V, 25 mA maximum	–	–	–

a. If you want to access this port for debugging purposes, it is recommended that you use the EP354 serial adapter and EP335 serial cable; refer to the *DT9840 Series Getting Started Manual* for connection information and to the *DT9840 Series DSP Library User's Manual* for information on the serial debugging functions. If you want to program this serial port, refer to the data sheet for the TMS320C6713 from Texas Instruments for more information.

Table 16: USB Connector (J6) Pin Assignments

Pin	Signal Name	Cable Wire
1	+5V_USB[a]	Red
2	USB_D–	White
3	USB_D+	Green
4	AGND1	Black

a. This signal is not used; USB connector is type B.

Table 17: Power Input Connector (J11) Pin Assignments

Pin	Signal Description[a]
1	+5 V Input @ 6 A
2	+5 V Input @ 6 A
3	Isolated Power Ground
4	Isolated Power Ground

a. You must consider the wire size and length before connecting power to connector J11. The module requirement is +5 V ±0.25 V at the connector with less than 50 mV pp of ripple. The power supply must also be isolated from the computer or from the power commons up to 500 V minimum.

Table 18: Scalable Bus Connectors (J12 and J13) Pin Assignments

Pin	Signal Description[a]	Pin	Signal Description
2	SB0	1	SB0_Return
4	SB1	3	SB1_Return
6	SB2	5	SB2_Return
8	SB3	7	SB3_Return
10	SB4	9	SB4_Return
12	SB5	11	SB5_Return
14	SB6	13	SB6_Return
16	SB7	15	SB7_Return
18	SB8	17	SB8_Return
20	SB9	19	SB9_Return
22	SB10	21	SB10_Return
24	SB11	23	SB11_Return

Table 18: Scalable Bus Connectors (J12 and J13) Pin Assignments (cont.)

Pin	Signal Description[a]	Pin	Signal Description
26	SB12	25	SB12_Return
28	SB13	27	SB13_Return
30	SB14	29	SB14_Return
32	SB15	31	SB15_Return
34	SB_Strobe	33	SB_Strobe_Return
36	Isolated Common	35	Isolated Common
38	Module Address Select 0	37	Module Address Select 1
40	Module Address Select 2	39	Module Address Select 3
42	Broadcast	41	SB Enable
44	SB Read/Write_L	43	Done_L
46	Master Serial Port 0 Data	45	Master Serial Port 0 Clock
48	Left/Right Clock	47	Isolated Common
50	Master ADClock	49	Master A/D Clock_L

a. The Scalable Bus connectors are set up for intermodule communication at speeds up to 50 MBytes/s (maximum software rate is 13 MBytes/s). The first and last modules must use software-selectable 100 Ω termination resistors. The data can be clocked out every 40 ns. The negative strobe pulse must be 12 ns minimum with the data valid for 10 ns before the rising edge. The hold time is 0 ns.

Table 19: Analog Output, Digital I/O, and Counter/Timer Connector (J17) Pin Assignments

Pin	Signal Description	Pin	Signal Description
34	Analog Output 00	68	Analog Output 00 Return
33	Analog Output 01	67	Analog Output 01 Return
32	Analog Output 02[a]	66	Analog Output 02 Return[a]
31	Analog Output 03[a]	65	Analog Output 03 Return[a]
30	Analog Output 04[a]	64	Analog Output 04 Return[a]
29	Analog Output 05[a]	63	Analog Output 05 Return[a]
28	Analog Output 06[a]	62	Analog Output 06 Return[a]
27	Analog Output 07[a]	61	Analog Output 07 Return[a]
26	External D/A Trigger[b]	60	Isolated Digital Ground
25	External D/A Clock[b]	59	Isolated Digital Ground
24	External A/D Trigger[b]	58	Isolated Digital Ground
23	External A/D Clock[b]	57	Isolated Digital Ground
22	Digital Input Trigger[b]	56	Isolated Digital Ground
21	Digital Input Clock[b]	55	Isolated Digital Ground
20	Digital Output Trigger[b]	54	Isolated Digital Ground
19	Digital Output Clock[b]	53	Isolated Digital Ground
18	Digital Input/Output 3, Port 0	52	Digital Input/Output 7, Port 0
17	Digital Input/Output 2, Port 0	51	Digital Input/Output 6, Port 0
16	Digital Input/Output 1, Port 0	50	Digital Input/Output 5, Port 0
15	Digital Input/Output 0, Port 0	49	Digital Input/Output 4, Port 0
14	Digital Input/Output 3, Port 1	48	Digital Input/Output 7, Port 1
13	Digital Input/Output 2, Port 1	47	Digital Input/Output 6, Port 1

Table 19: Analog Output, Digital I/O, and Counter/Timer Connector (J17) Pin Assignments (cont.)

Pin	Signal Description	Pin	Signal Description
12	Digital Input/Output 1, Port 1	46	Digital Input/Output 5, Port 1
11	Digital Input/Output 0, Port 1	45	Digital Input/Output 4, Port 1
10	Digital Input/Output 3, Port 2/ TINP1[b]	44	Digital Input/Output 7, Port 2
9	Digital Input/Output 2, Port 2/ Encoder 2 Clr[b]	43	Digital Input/Output 6, Port 2
8	Digital Input/Output 1, Port 2/ Encoder 1 Clr[b]	42	Digital Input/Output 5, Port 2
7	Digital Input/Output 0, Port 2/ Encoder 0 Clr[b]	41	Digital Input/Output 4, Port 2
6	User Clock Input 0/ Encoder A0[b]	40	Isolated Digital Ground
5	User Counter Output 0	39	External Gate 0/ Encoder B0[b]
4	User Clock Input 1/ Encoder A1[b]	38	Isolated Digital Ground
3	User Counter Output 1	37	External Gate 1/ Encoder B1[b]
2	User Clock Input 2/ Encoder A2[b]	36	Isolated Digital Ground
1	User Counter Output 2	35	External Gate 2/ Encoder B2[b]

a. Available on the DT9842/8 module only.
b. Currently, this function is not implemented.

Table 20: Analog Input Connector (J18) Pin Assignments

Pin	Signal Description	Pin	Signal Description
34	Analog Input 00	68	Analog Input 00 Return[a]
33	Analog Input 01	67	Analog Input 01 Return[a]
32	Analog Input 02	66	Analog Input 02 Return[a]
31	Analog Input 03	65	Analog Input 03 Return[a]
30	Analog Input 04	64	Analog Input 04 Return[a]
29	Analog Input 05	63	Analog Input 05 Return[a]
28	Analog Input 06	62	Analog Input 06 Return[a]
27	Analog Input 07	61	Analog Input 07 Return[a]
26	Reserved	60	Reserved
25	Reserved	59	Reserved
24	Reserved	58	Reserved
23	Reserved	57	Reserved
22	Reserved	56	Reserved
21	Reserved	55	Reserved
20	Reserved	54	Reserved
19	Reserved	53	Reserved
18	Reserved	52	Reserved
17	Reserved	51	Reserved
16	Reserved	50	Reserved
15	Reserved	49	Reserved
14	Reserved	48	Reserved
13	Reserved	47	Reserved
12	Reserved	46	Reserved

Table 20: Analog Input Connector (J18) Pin Assignments (cont.)

Pin	Signal Description	Pin	Signal Description
11	Reserved	45	Reserved
10	Reserved	44	Reserved
9	Reserved	43	Reserved
8	Reserved	42	Reserved
7	Reserved	41	Reserved
6	Reserved	40	Reserved
5	Reserved	39	Reserved
4	Reserved	38	Reserved
3	Reserved	37	Reserved
2	Amp Low	36	Analog Common
1	+5 V Isolated Output	35	Isolated Power Ground

a. For the DT9842/2 and DT9842/8, which have single-ended analog inputs, these signals are analog grounds.

Table 21: Power Output Connector (J19) Pin Assignments

Pin	Signal Description
1	+5 V Output @ 1 A[a]
2	Isolated Power Ground

a. Fused at 1 A with a poly fuse.

Table 22: Power Output Screw Terminal Block (TB1)

Pin	Signal Description
1	+5 V Output @ 1 A[a]
2	Isolated Power Ground

a. Fused at 1 A with a poly fuse.

DT9841E Module

The DT9841E module provides the following connectors:

- Connector J1 – a 68-pin connector provided for attaching analog output, digital I/O, and counter/timer signals, as well as an external clock and external trigger input. Refer to Table 23 on page 159 for more information on this connector.
- Connector J2 – a 68-pin connector provided for attaching analog input signals. Refer to Table 24 on page 162 for more information on this connector.
- Connector J3 – a 14-pin connector provided for a JTAG device, such as a Blackhawk emulator. Refer to Table 25 on page 163 for more information on this connector.
- Connector J4 – a 10-pin, D-shell connector provided for attaching an RS-232-compliant device for debugging purposes using the EP368 cable, EP354 serial adapter, and EP335 cable. Refer to the *DT9840 Series Getting Started Manual* for connection information and to the *DT9840 Series DSP Library User's Manual* for information about the serial debugging functions.

Note: When used with the EP368, the J4 connector provides the pin assignments shown in Table 26 on page 164.

This serial port (serial port 1 (McBSP) of the DSP) can also be programmed for several modes of operation at bit rates of up to 33 Mbps. Refer to the data sheet for the TMS320C6713 from Texas Instruments (part number SPRS088F) for more information on programming the serial port.

- Connector J6 – a 4-pin USB connector. Refer to Table 27 on page 165 for more information on this connector.
- Connector J11 – a 4-pin locking connector provided for attaching an external +5 V power input signal. Refer to Table 28 on page 165 for more information on this connector.

Note: You must consider the wire size and length before connecting power to connector J11. The module requirement is +5 V ±0.25 V at the connector with less than 50 mV pp of ripple. The power supply must also be isolated from the computer or from the power commons up to 500 V minimum. The following power supply is recommended: Total Power International number TPES49-05060KPP-4P or Data Translation EP348 (part number 19481).

- Screw Terminal Block TB2 – a 3-position screw terminal block provided for attaching a +5 V power supply. You can use this screw terminal block instead of connector J11 to provide power to the module. Refer to Table 29 on page 166 for more information on this screw terminal block.

- Screw Terminal Block TB3– a 2-position screw terminal block provided for attaching an external +5 VDC, 100 mA fan output signal. The fan will turn on with an onboard temperature sensor if the DT9841E module exceeds 45° C. If the module exceeds 60° C, an interrupt is generated. The following fan is recommended: Sunon model number KDE0505PFB3-8GN or Data Translation part number 19372. Refer to Table 30 on page 166 for more information on this screw terminal block.

Table 23: Analog Output, Digital I/O, Counter/Timer, Ext Trig, Ext Clock Connector (J1) Pin Assignments on the DT9841E

Pin	Signal Description	Pin	Signal Description
34	Analog Output 00	68	Analog Output 00 Return
33	Analog Output 01	67	Analog Output 01 Return
32	Reserved	66	Reserved
31	Reserved	65	Reserved
30	Reserved	64	Reserved
29	Reserved	63	Reserved
28	Reserved	62	Reserved
27	Reserved	61	Reserved
26	External D/A Trigger[a]	60	Isolated Digital Ground
25	External D/A Clock[a]	59	Isolated Digital Ground
24	External A/D Trigger[b]	58	Isolated Digital Ground
23	External A/D Clock[c]	57	Isolated Digital Ground
22	Digital Input Trigger[a]	56	Isolated Digital Ground
21	Digital Input Clock[a]	55	Isolated Digital Ground
20	Digital Output Trigger[a]	54	Isolated Digital Ground
19	Digital Output Clock[a]	53	Isolated Digital Ground

Table 23: Analog Output, Digital I/O, Counter/Timer, Ext Trig, Ext Clock Connector (J1) Pin Assignments on the DT9841E (cont.)

Pin	Signal Description	Pin	Signal Description
18	Digital Input/Output 3, Port 0	52	Digital Input/Output 7, Port 0
17	Digital Input/Output 2, Port 0	51	Digital Input/Output 6, Port 0
16	Digital Input/Output 1, Port 0	50	Digital Input/Output 5, Port 0
15	Digital Input/Output 0, Port 0	49	Digital Input/Output 4, Port 0
14	Digital Input/Output 3, Port 1	48	Digital Input/Output 7, Port 1
13	Digital Input/Output 2, Port 1	47	Digital Input/Output 6, Port 1
12	Digital Input/Output 1, Port 1	46	Digital Input/Output 5, Port 1
11	Digital Input/Output 0, Port 1	45	Digital Input/Output 4, Port 1
10	Digital Input/Output 3, Port 2/ TINP1[a]	44	Digital Input/Output 7, Port 2
9	Digital Input/Output 2, Port 2/ Encoder 2 Clr[a]	43	Digital Input/Output 6, Port 2
8	Digital Input/Output 1, Port 2/ Encoder 1 Clr[a]	42	Digital Input/Output 5, Port 2
7	Digital Input/Output 0, Port 2/ Encoder 0 Clr[a]	41	Digital Input/Output 4, Port 2
6	User Clock Input 0/ Encoder A0[a]	40	Isolated Digital Ground
5	User Counter Output 0	39	External Gate 0/ Encoder B0[a]
4	User Clock Input 1/ Encoder A1[a]	38	Isolated Digital Ground

Table 23: Analog Output, Digital I/O, Counter/Timer, Ext Trig, Ext Clock Connector (J1) Pin Assignments on the DT9841E (cont.)

Pin	Signal Description	Pin	Signal Description
3	User Counter Output 1	37	External Gate 1/ Encoder B1[a]
2	User Clock Input 2/ Encoder A2[a]	36	Isolated Digital Ground
1	User Counter Output 2	35	External Gate 2/ Encoder B2[a]

a. Currently, this function is not implemented.
b. Use this pin to connect an external trigger to the DT9841E module.
c. Use this pin to connect an external clock to the DT9841E module.

Table 24: Analog Input Connector (J2) Pin Assignments on the DT9841E

Pin	Signal Description	Pin	Signal Description
34	Analog Input 00	68	Analog Input 00 Return
33	Analog Input 01	67	Analog Input 01 Return
32	Reserved	66	Reserved
31	Reserved	65	Reserved
30	Reserved	64	Reserved
29	Reserved	63	Reserved
28	Reserved	62	Reserved
27	Reserved	61	Reserved
26	Reserved	60	Reserved
25	Reserved	59	Reserved
24	Reserved	58	Reserved
23	Reserved	57	Reserved
22	Reserved	56	Reserved
21	Reserved	55	Reserved
20	Reserved	54	Reserved
19	Reserved	53	Reserved
18	Reserved	52	Reserved
17	Reserved	51	Reserved
16	Reserved	50	Reserved
15	Reserved	49	Reserved
14	Reserved	48	Reserved
13	Reserved	47	Reserved
12	Reserved	46	Reserved

Table 24: Analog Input Connector (J2) Pin Assignments on the DT9841E

Pin	Signal Description	Pin	Signal Description
11	Reserved	45	Reserved
10	Reserved	44	Reserved
9	Reserved	43	Reserved
8	Reserved	42	Reserved
7	Reserved	41	Reserved
6	Reserved	40	Reserved
5	Reserved	39	Reserved
4	Reserved	38	Reserved
3	Reserved	37	Reserved
2	Amp Low	36	Analog Common
1	+5 V Isolated Output	35	Isolated Power Ground

Table 25: JTAG Connector (J3) Pin Assignments on the DT9841E

Pin	Signal Name	Pin	Signal Name
1	DSP_TMS	2	DSP_TRST_N
3	DSP_TDI	4	DGND
5	+3.3 V	6	Not Connected
7	DSP_TDO	8	DGND
9	DSP_TCK	10	DGND
11	DSP_TCK	12	DGND
13	DSP_EMU0	14	DSP_EMU1

Table 26: Serial Port Connector (J4) Pin Assignments on the DT9841E

J4. Pin	Signal Name[a]	Signal Description	McBSP Pin	McBSP Function	McBSP Internal Pull Up or Pull Down
1	CLKS1	External Clock Source	E1	Input	Internal Pull Down
2	CLKX1	Transmit Clock	L3	Input/Output/ Tristate	Internal Pull Down
3	DR1	Receive Data	M2	Input	Internal Pull Up
4	FSX1	Transmit Frame Sync	L1	Input/Output/ Tristate	Internal Pull Down
5	DX1	Transmit Data	L2	Output/ Tristate	Internal Pull Up
6	FSR1	Receive Frame Sync	M3	Input/Output/ Tristate	Internal Pull Down
7	CLKR1	Receive Clock	M1	Input/Output/ Tristate	Internal Pull Down
8	+5 V_PWR	+5 V, 25 mA maximum	–	–	–
9	Digital Ground	Ground	–	–	–
10	Digital Ground	Ground	–	–	–

a. If you want to access this port for debugging purposes, it is recommended that you use the EP354 serial adapter and EP335 serial cable; refer to the *DT9840 Series Getting Started Manual* for connection information and to the *DT9840 Series DSP Library User's Manual* for information on the serial debugging functions. If you want to program this serial port, refer to the data sheet for the TMS320C6713 from Texas Instruments for more information.

Table 27: USB Connector (J6) Pin Assignments on the DT9841E

Pin	Signal Name	Cable Wire
1	+5V_USB[a]	Red
2	USB_D–	White
3	USB_D+	Green
4	AGND1	Black

a. This signal is not used; USB connector is type B.

Table 28: Power Input Connector (J11) Pin Assignments on the DT9841E

Pin	Signal Description[a]
1	+5 V Input @ 6 A
2	+5 V Input @ 6 A
3	Isolated Power Ground
4	Isolated Power Ground

a. You must consider the wire size and length before connecting power to connector J11. The module requirement is +5 V ±0.25 V at the connector with less than 50 mV pp of ripple. The power supply must also be isolated from the computer or from the power commons up to 500 V minimum.

Table 29: Secondary Power Connector (TB2) Screw Terminal Assignments on the DT9841E

Screw Terminal	Signal Name
1	+5 V Input
2	Ground
3	Chassis Ground

Table 30: Fan Output Connector (TB3) Screw Terminal Assignments on the DT9841E

Screw Terminal	Signal Name[a]
1	Fan+
2	Fan–

a. These signals are provided for attaching an external +5 VDC, 100 mA fan output signal. The fan will turn on with an onboard temperature sensor if the DT9840 Series module exceeds 45° C. If the module exceeds 60° C, an interrupt is generated. The following fan is recommended: Sunon model number KDE0505PFB3-8GN or Data Translation part number 19372.

Sleek Box Front Panel

The following connectors are provided on the front panel of the Sleek Box:

- **BNC connectors** – BNCs labelled AD Ch0 to AD Ch7 are provided for attaching eight analog input signals. The BNCs are wired on the box to reflect the channel configuration (single-ended or differential) of your module.

  On the DT9841 and DT9842/2 Sleek Box, BNCs labelled DAC Ch0 to DAC Ch3 are provided for attaching four analog output signals. On the DT9842/8, BNCs labelled DAC Ch0 to DAC Ch7 are provided for attaching eight analog output signals.

  The BNC labelled TTL Clock is provided for attaching an external clock signal. The BNC labelled TTL Trigger is provided for attaching an external trigger signal.

- **Analog In/Out Connector (J1)** – A 37-pin connector provided for attaching analog I/O signals. Refer to Table 31 on page 168 for more information on this connector.

- **Digital In/Out Connector (J2)** – A 37-pin connector provided for attaching digital I/O signals. Refer to Table 32 on page 169 for more information on this connector.

- **Counter Timer Connector (J19)** – A 25-pin connector provided for attaching counter/timer signals. Refer to Table 33 on page 171 for more information on this connector.

- **Screw terminal block** – A screw terminal block is provided for attaching an external +5 V power output signal. Table 22 on page 157 for more information on this screw terminal block.

The back panel of the Sleek Box provides these connectors:

- **Scalable Bus Connectors (J12 and J13)** – Refer to Table 18 on page 151 for the pin assignments of these connectors.
- **Serial Port (J4)** – Refer to Table 15 on page 149 for the pin assignments of this connector.
- **+5 V Power Input Connector (J11)** – Refer to Table 17 on page 151 for the pin assignments of this connector.
- **USB connector (J6)** – Refer to Table 16 on page 150 for the pin assignments of this connector.

Table 31: Analog In/Out Connector (J1) Pin Assignments on the Sleek Box

J1 Pin Assignment	Signal Description	J1 Pin Assignment	Signal Description
1	Analog Input 00	2	Analog Input 01
3	Analog Input 02	4	Analog Input 03
5	Analog Input 04	6	Analog Input 05
7	Analog Input 06	8	Analog Input 07
9	Analog Common	10	Analog Output 00
11	Analog Output 01	12	Analog Output 02[a]
13	Analog Output 03[a]	14	Analog Output 04[a]
15	Analog Output 05[a]	16	Analog Output 06[a]
17	Analog Output 07[a]	18	Analog Common
19	Reserved	20	Analog Input 00 Return[b]
21	Analog Input 01 Return[b]	22	Analog Input 02 Return[b]
23	Analog Input 03 Return[b]	24	Analog Input 04 Return[b]
25	Analog Input 05 Return[b]	26	Analog Input 06 Return[b]
27	Analog Input 07 Return[b]	28	Analog Common

Table 31: Analog In/Out Connector (J1) Pin Assignments on the Sleek Box

J1 Pin Assignment	Signal Description	J1 Pin Assignment	Signal Description
29	Analog Output 00 Return	30	Analog Output 01 Return
31	Analog Output 02 Return[a]	32	Analog Output 03 Return[a]
33	Analog Output 04 Return[a]	34	Analog Output 05 Return[a]
35	Analog Output 06 Return[a]	36	Analog Output 07 Return[a]
37	Analog Common		

a. Available on the DT9842/8 module only. For all other modules, these signals are reserved.
b. For the DT9841-VIB, DT9842/2 and DT9842/8, which have single-ended analog inputs, these signals are analog grounds.

Table 32: Digital In/Out Connector (J2) Pin Assignments on the Sleek Box

J2 Pin Assignment	Signal Description	J2 Pin Assignment	Signal Description
1	Digital In/Out 3, Port 0	2	Digital In/Out 2, Port 0
3	Digital In/Out 1, Port 0	4	Digital In/Out 0, Port 0
5	Digital In/Out 3, Port 1	6	Digital In/Out 2, Port 1
7	Digital In/Out 1, Port 1	8	Digital In/Out 0, Port 1
9	Digital In/Out 3, Port 2[a]/ TINP1[b]	10	Digital In/Out 2, Port 2[a]/ Encoder 2 Clr[b]
11	Digital In/Out 1, Port 2[a]/ Encoder 1 Clr[b]	12	Digital In/Out 0, Port 2[a]/ Encoder 0 Clr[ab]
13	Isolated Digital Ground	14	Isolated Digital Ground

Table 32: Digital In/Out Connector (J2) Pin Assignments on the Sleek Box (cont.)

J2 Pin Assignment	Signal Description	J2 Pin Assignment	Signal Description
15	Isolated Digital Ground	16	Isolated Digital Ground
17	Isolated Digital Ground	18	Isolated Digital Ground
19	Reserved	20	Digital In/Out 7, Port 0
21	Digital In/Out 6, Port 0	22	Digital In/Out 5, Port 0
23	Digital In/Out 4, Port 0	24	Digital In/Out 7, Port 1
25	Digital In/Out 6, Port 1	26	Digital In/Out 5, Port 1
27	Digital In/Out 4, Port 1	28	Digital In/Out 7, Port 2[a]
29	Digital In/Out 6, Port 2[a]	30	Digital In/Out 5, Port 2[a]
31	Digital In/Out 4, Port 2[a]	32	Isolated Digital Ground
33	Isolated Digital Ground	34	Isolated Digital Ground
35	Isolated Digital Ground	36	Isolated Digital Ground
37	Isolated Digital Ground		

a. Port 2 is not supported on the DT9841-VIB; these signals are reserved for the DT9841-VIB.
b. Currently, not implemented.

Table 33: Counter/Timer Connector (J19) Pin Assignments on the Sleek Box

J13 Pin Assignment	Signal Description	J13 Pin Assignment	Signal Description
1	User Counter Output 2	2	User Clock Input 2/ Encoder A2[a]
3	User Counter Output 1	4	User Clock Input 1/ Encoder A1[a]
5	User Counter Output 0	6	User Clock Input 0/ Encoder A0[a]
7	Isolated Digital Ground	8	Isolated Digital Ground
9	Isolated Digital Ground	10	Isolated Digital Ground
11	Isolated Digital Ground	12	Isolated Digital Ground
13	Reserved	14	External Gate 2/ Encoder B2[a]
15	Isolated Digital Ground	16	External Gate 1/ Encoder B1[a]
17	Isolated Digital Ground	18	External Gate 0/ Encoder B0[a]
19	Isolated Digital Ground	20	Isolated Digital Ground
21	Isolated Digital Ground	22	Isolated Digital Ground
23	Isolated Digital Ground	24	Isolated Digital Ground
25	Isolated Digital Ground		

a. Currently, the encoder signals are not implemented.

EP358E Accessory Panel

The EP358E accessory panel is provided for DT9841E modules. The following connectors are provided on the front of the EP358E accessory panel:

- **BNC connectors** –BNCs labelled CH0 and CH1 are provided for attaching two differential analog input signals.
- **Analog In/Out Connector (J1)** –A 37-pin connector provided for attaching analog I/O signals. Refer to Table 31 on page 168 for more information on this connector.
- **Digital In/Out Connector (J2)** –A 37-pin connector provided for attaching digital I/O signals. Refer to Table 32 on page 169 for more information on this connector.
- **Counter Timer Connector (J19)** –A 25-pin connector provided for attaching counter/timer signals. Refer to Table 33 on page 171 for more information on this connector.

The back of the EP358E accessory panel provides these connectors:

- **J202 Connector** –68-pin connector for connecting the EP358E accessory panel to the J2 connector of the DT9841E module. This connector brings out all the analog input signals from the module to the accessory panel.
- **J201 Connector** –68-pin connector for connecting the EP358E accessory panel to the J1 connector of the DT9841E module. This connector brings out all of the analog output, digital I/O, and counter/timer signals, as well as an external clock and external trigger input signals from the module to the accessory panel.

Table 34: Pin Assignments for Connector J202 on the EP358E Accessory Panel

Pin	Signal Description	Pin	Signal Description
1	+5 V Isolated Output	2	Amp Low
3	Reserved	4	Reserved
5	Reserved	6	Reserved
7	Reserved	8	Reserved
9	Reserved	10	Reserved
11	Reserved	12	Reserved
13	Reserved	14	Reserved
15	Reserved	16	Reserved
17	Reserved	18	Reserved
19	Reserved	20	Reserved
21	Reserved	22	Reserved
23	Reserved	24	Reserved
25	Reserved	26	Reserved
27	Reserved	28	Reserved
29	Reserved	30	Reserved
31	Reserved	32	Reserved
33	Analog Input 01	34	Analog Input 00
35	Isolated Power Ground	36	Analog Common
37	Reserved	38	Reserved
39	Reserved	40	Reserved
41	Reserved	42	Reserved
43	Reserved	44	Reserved

Table 34: Pin Assignments for Connector J202 on the EP358E Accessory Panel (cont.)

Pin	Signal Description	Pin	Signal Description
45	Reserved	46	Reserved
47	Reserved	48	Reserved
49	Reserved	50	Reserved
51	Reserved	52	Reserved
53	Reserved	54	Reserved
55	Reserved	56	Reserved
57	Reserved	58	Reserved
59	Reserved	60	Reserved
61	Reserved	62	Reserved
63	Reserved	64	Reserved
65	Reserved	66	Reserved
67	Analog Input 01 Return	68	Analog Input 00 Return

Table 35: Pin Assignments for Connector J201 on the EP358E Accessory Panel

Pin	Signal Description	Pin	Signal Description
1	User Counter Output 2	2	User Clock Input 2/ Encoder A2[a]
3	User Counter Output 1	4	User Clock Input 1/ Encoder A1[a]
5	User Counter Output 0	6	User Clock Input 0/ Encoder A0[a]

Table 35: Pin Assignments for Connector J201 on the EP358E Accessory Panel

Pin	Signal Description	Pin	Signal Description
7	Digital Input/Output 0, Port 2/ Encoder 0 Clr[a]	8	Digital Input/Output 1, Port 2/ Encoder 1 Clr[a]
9	Digital Input/Output 2, Port 2/ Encoder 2 Clr[a]	10	Digital Input/Output 3, Port 2/ TINP1[a]
11	Digital Input/Output 0, Port 1	12	Digital Input/Output 1, Port 1
13	Digital Input/Output 2, Port 1	14	Digital Input/Output 3, Port 1
15	Digital Input/Output 0, Port 0	16	Digital Input/Output 1, Port 0
17	Digital Input/Output 2, Port 0	18	Digital Input/Output 3, Port 0
19	Digital Output Clock[a]	20	Digital Output Trigger[a]
21	Digital Input Clock[a]	22	Digital Input Trigger[a]
23	External A/D Clock[a]	24	External A/D Trigger[a]
25	External D/A Clock[a]	26	External D/A Trigger[a]
27	Reserved	28	Reserved
29	Reserved	30	Reserved
31	Reserved	32	Reserved
33	Analog Output 01	34	Analog Output 00
35	External Gate 2/ Encoder B2[a]	36	Isolated Digital Ground
37	External Gate 1/ Encoder B1[a]	38	Isolated Digital Ground
39	External Gate 0 Encoder B0[a]	40	Isolated Digital Ground
41	Digital Input/Output 4, Port 2	42	Digital Input/Output 5, Port 2
43	Digital Input/Output 6, Port 2	44	Digital Input/Output 7, Port 2

Table 35: Pin Assignments for Connector J201 on the EP358E Accessory Panel

Pin	Signal Description	Pin	Signal Description
45	Digital Input/Output 4, Port 1	46	Digital Input/Output 5, Port 1
47	Digital Input/Output 6, Port 1	48	Digital Input/Output 7, Port 1
49	Digital Input/Output 4, Port 0	50	Digital Input/Output 5, Port 0
51	Digital Input/Output 6, Port 0	52	Digital Input/Output 7, Port 0
53	Isolated Digital Ground	54	Isolated Digital Ground
55	Isolated Digital Ground	56	Isolated Digital Ground
57	Isolated Digital Ground	58	Isolated Digital Ground
59	Isolated Digital Ground	60	Isolated Digital Ground
61	Reserved	62	Reserved
63	Reserved	64	Reserved
65	Reserved	66	Reserved
67	Analog Output 01 Return	68	Analog Output 00 Return

a. Currently, not implemented.

Index

D

E

F

G

H

I

J

L

M

N

O

P

R

S

T

U

V

W

X